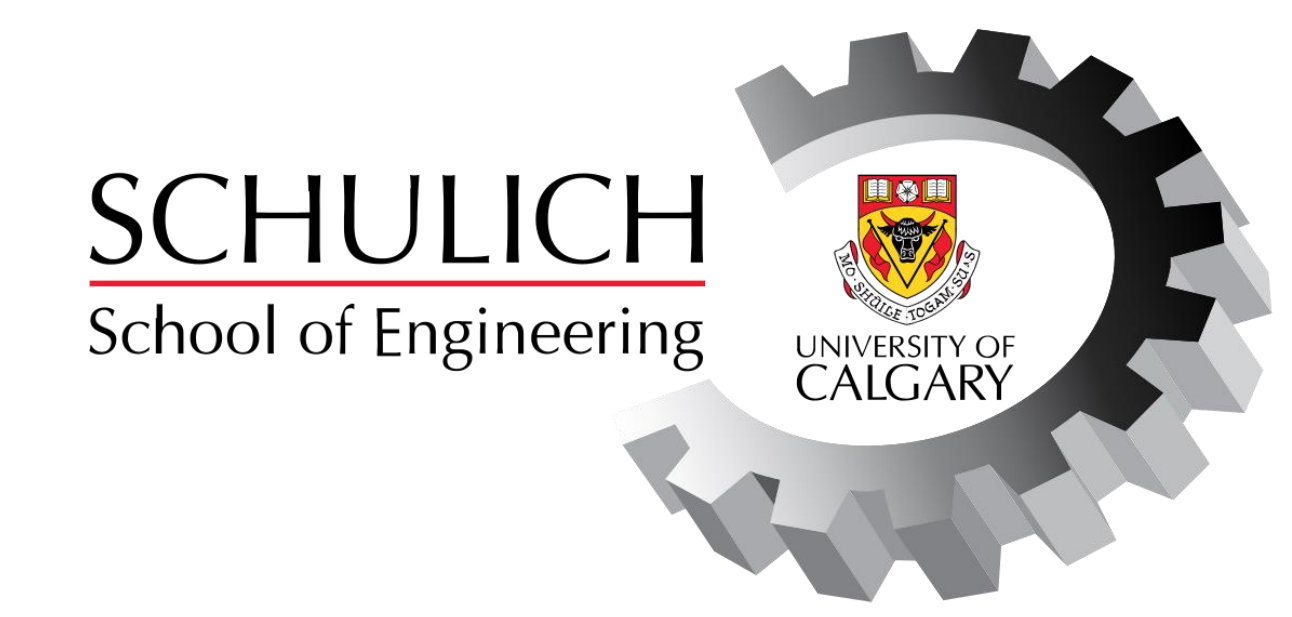
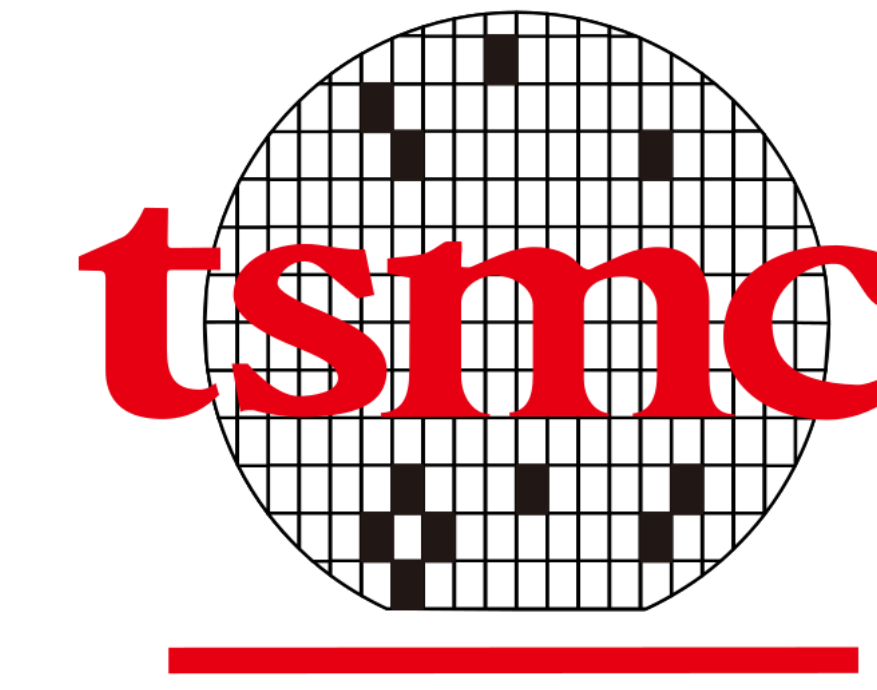


140 GHz Power Amplifier for 6G

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Abstract

This project aims to assess TSMC 65nm CMOS technology for millimetre wave wireless transmission and design a power amplifier for 136 to 142 GHz range. The amplifier boosts the signal power to drive an antenna in a 50 Ω environment, and deliverables include a system block diagram, schematic, and post-layout circuit parameters.

System Application

This project aims to develop power amplifiers that can operate in the THz range and enable 6G communication for IoT, AI, and data-intensive applications, with a focus on low-cost chip design.

To support the advanced sensor technologies in autonomous vehicles, high-speed wireless communications is required between the car's systems.



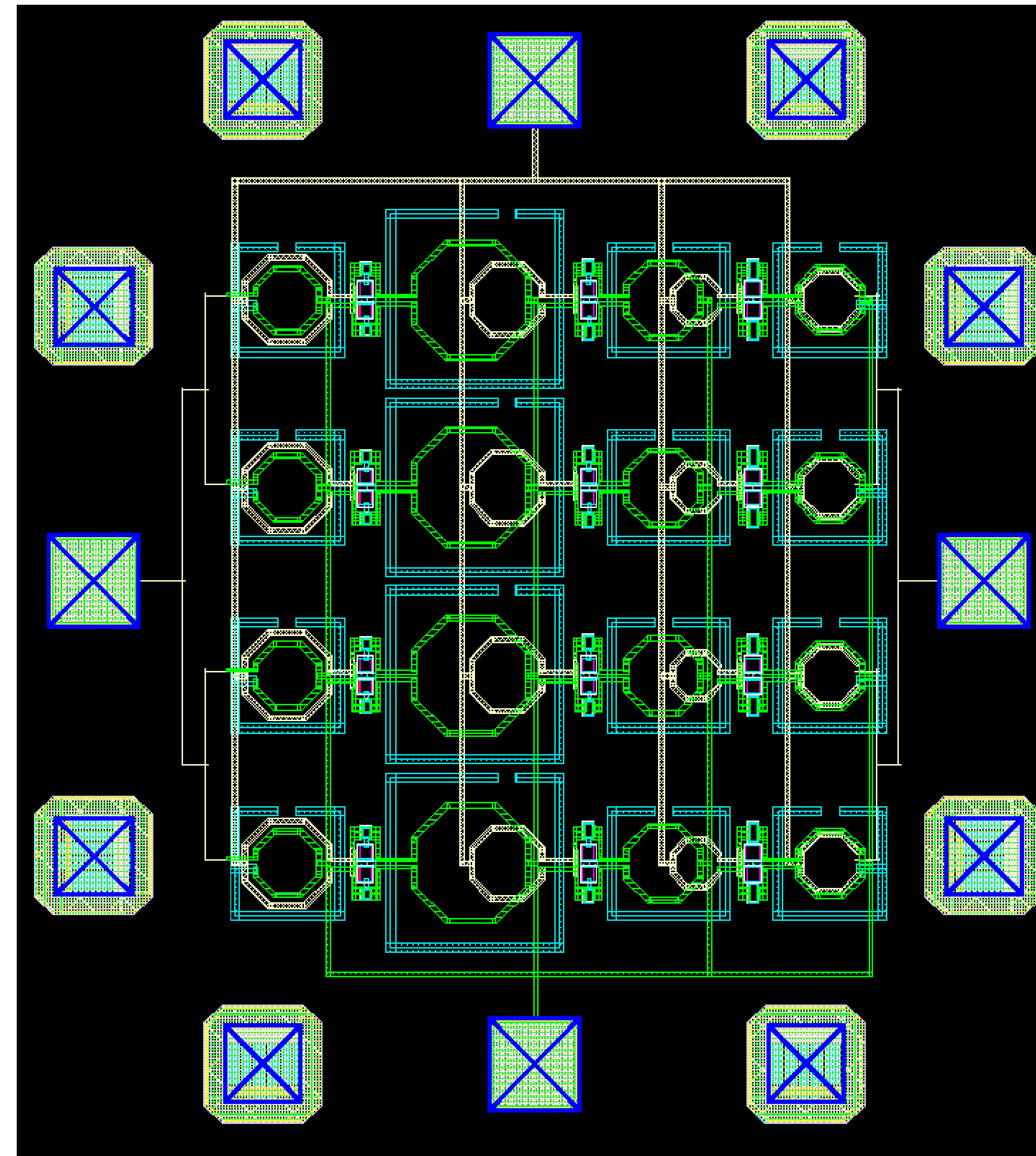
Figure 1: Autonomous Vehicles [1]

Efficient and optimized power amplifiers are important for low-power applications in IoT devices, such as sensors and wearables, to conserve battery power and minimize energy consumption.



Figure 2: Home Automation [2]

Power Amplifier

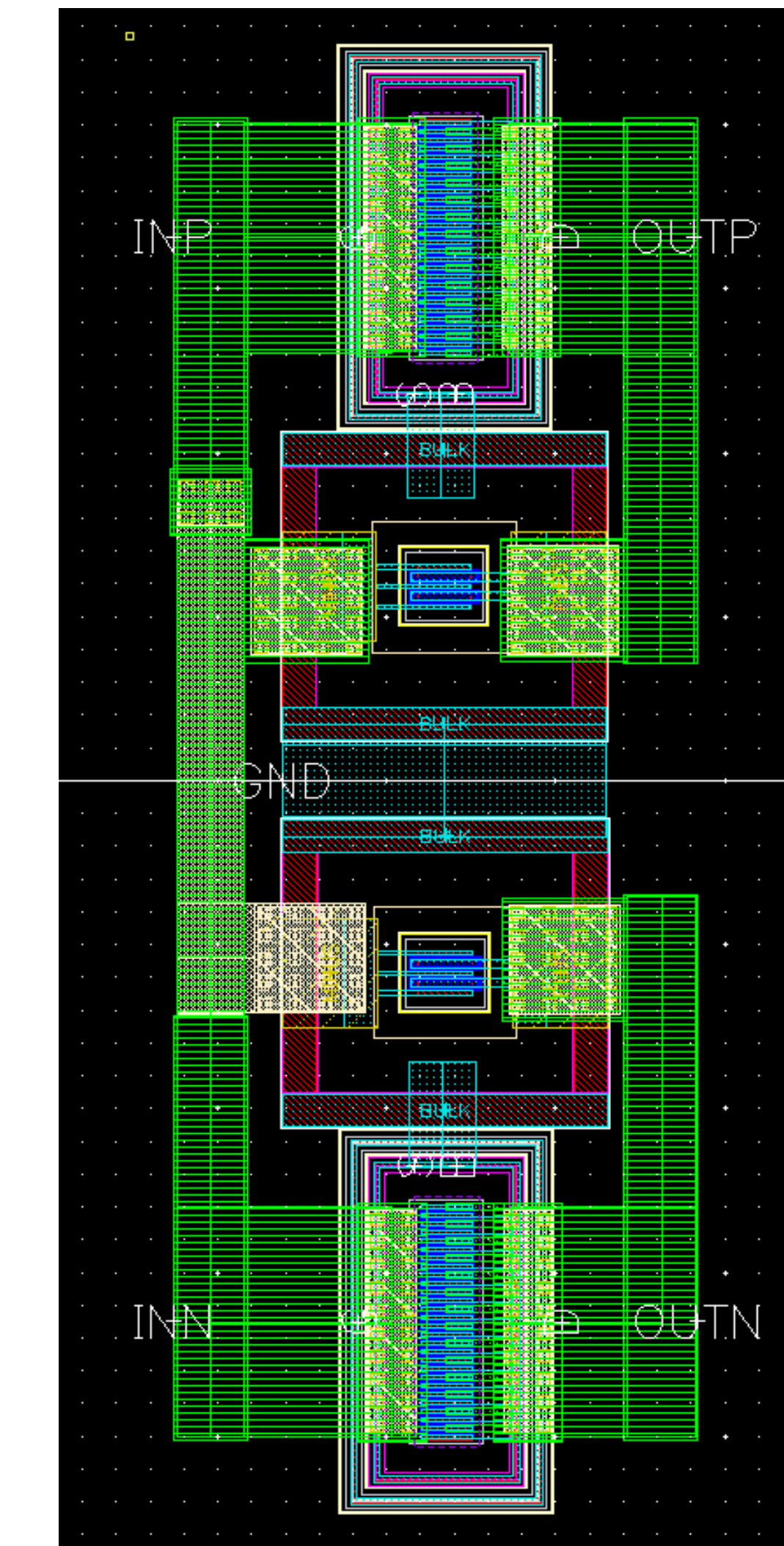


Our design includes both small and large transistor widths to ensure optimal impedance values for efficiency and power output. Once the amplifier core is selected, load pull analysis is conducted to determine the relationship between device width, power output, and optimum load impedance. This analysis helps to ensure that the amplifier meets the required gain and power specifications.

Transistor Width (μm)	Z_{opt} (R+jX)	OP1dB (dBm)	Psat (dBm)	Peak PAE (%)
20	32-j89	6	10	37
30	24-j63	9	13	51
40	20-j46	11	14	57
50	24-j44	11.498	15	44
60	18-j33	13	17	59

Transistor Width (μm)	$C_{neu,opt}$ (fF)	GMAX (dB) $C_{neu} = 0$	GMAX (dB) $C_{neu} = C_{neu,opt}$	1.5 dB Margin (dB)
10	3.2	7.3	8.5	7.0
20	5.6	7.6	7.2	5.7
30	8.4	5.6	6.2	4.7
40	11.0	4.4	5.2	4.0
50	12.0	3.6	4.4	3.2
60	14.0	3.1	3.8	2.6

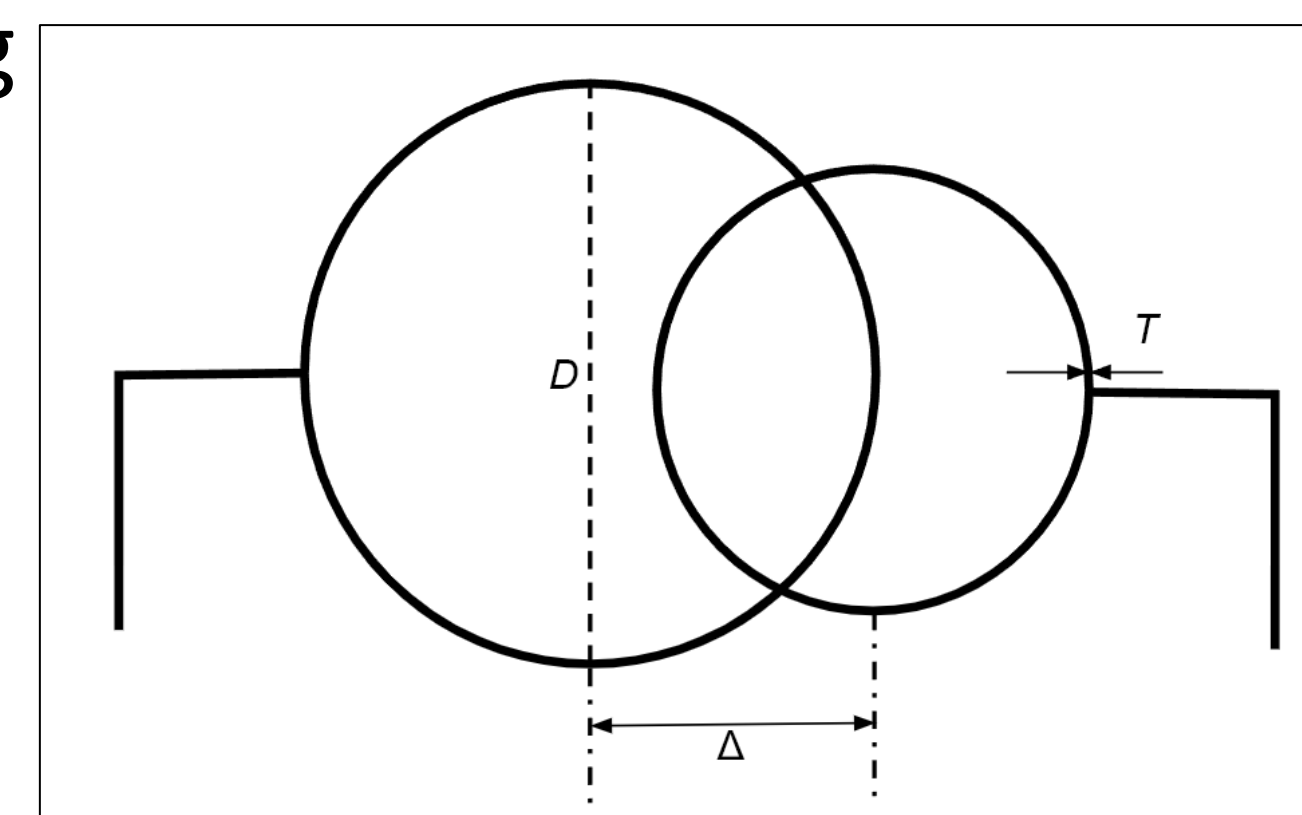
Power Amplifier Core



After a literature review, a capacitive neutralization design was used due to its simplicity and wideband operation. The custom core was designed in a way to minimize layer crossing, trace length and via usage all of which contribute to added losses and unwanted capacitances.

Transformer

Varying the parameters D (winding diameter), Delta (winding offset), and T (trace thickness) affects the transformer's inductance and coupling co-efficient, and the amplifier's overall gain and power output.



A comparison between our optimized values and simulated values are shown. Transformer inductances were varied to find which values provided the maximum gain, unconditional stability and optimum output impedance.

Transformer #	Lp (pH)	Ls (pH)	k
1	53.6	116.4	0.45
2	116.4	76.4	0.26
3	69.2	37.8	0.26
4	59.4	58.2	0.45

Transformer #	Lp (pH)	Ls (pH)	k
1	57.1	120.7	0.53
2	117.6	72.1	0.28
3	70.3	39.7	0.23
4	57.6	58.1	0.74

Power Combining

A zero-degree power combining layout was used to combine multiple stages for simplicity, minimal loss and size. By connecting each branch, individual power from each stage is summed up to simulate and test to power a design standard load of 50Ω.

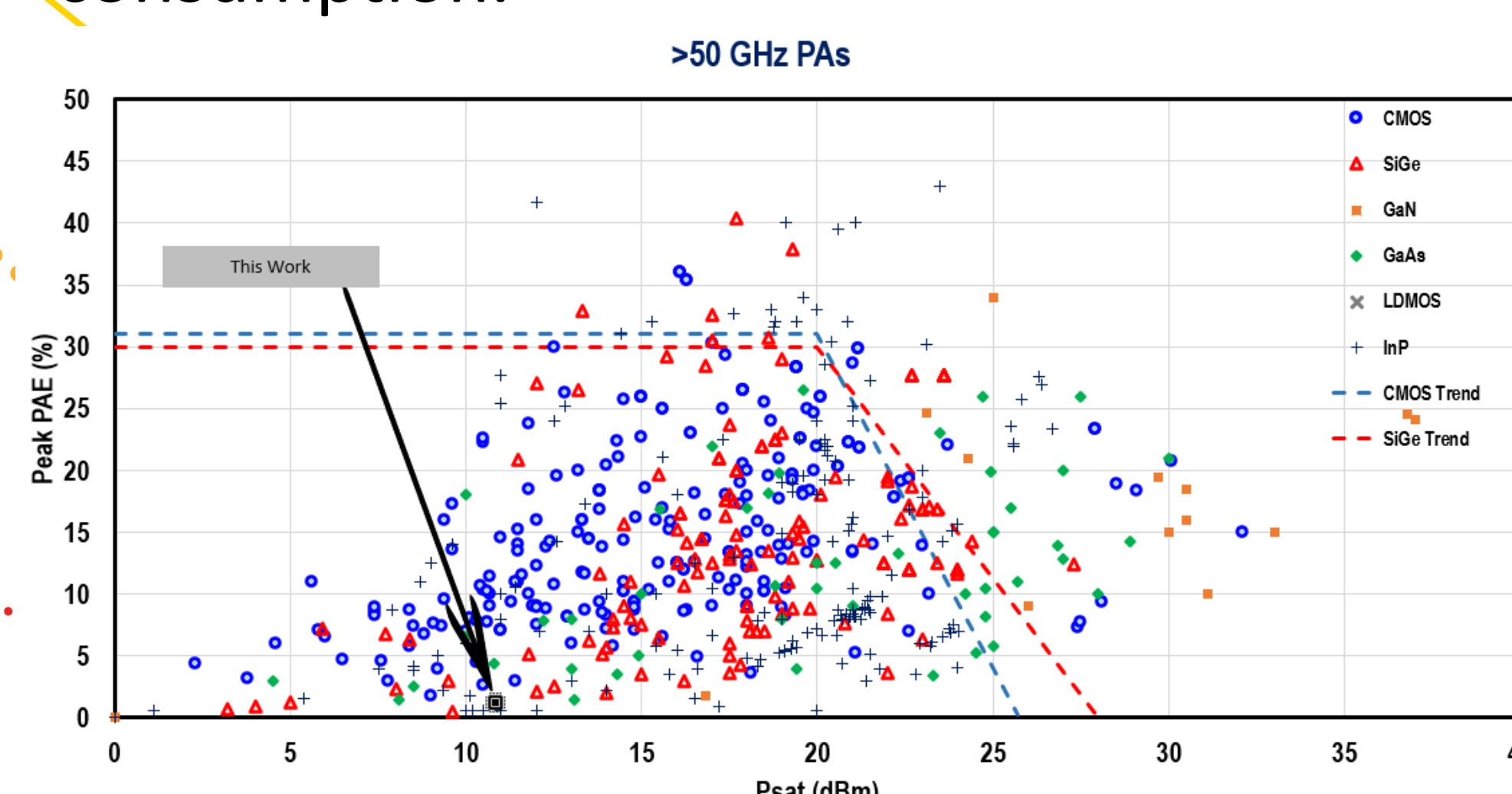
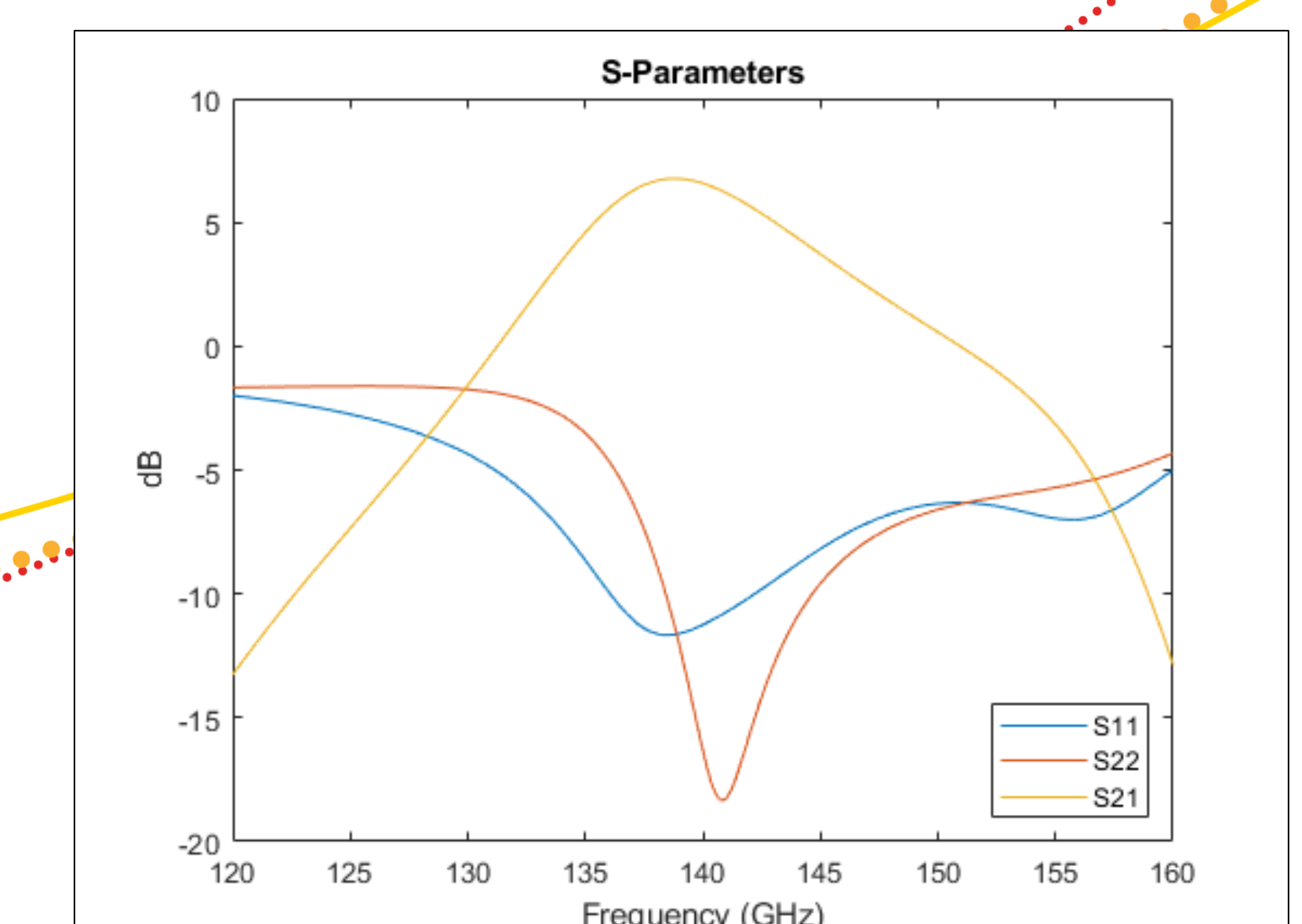
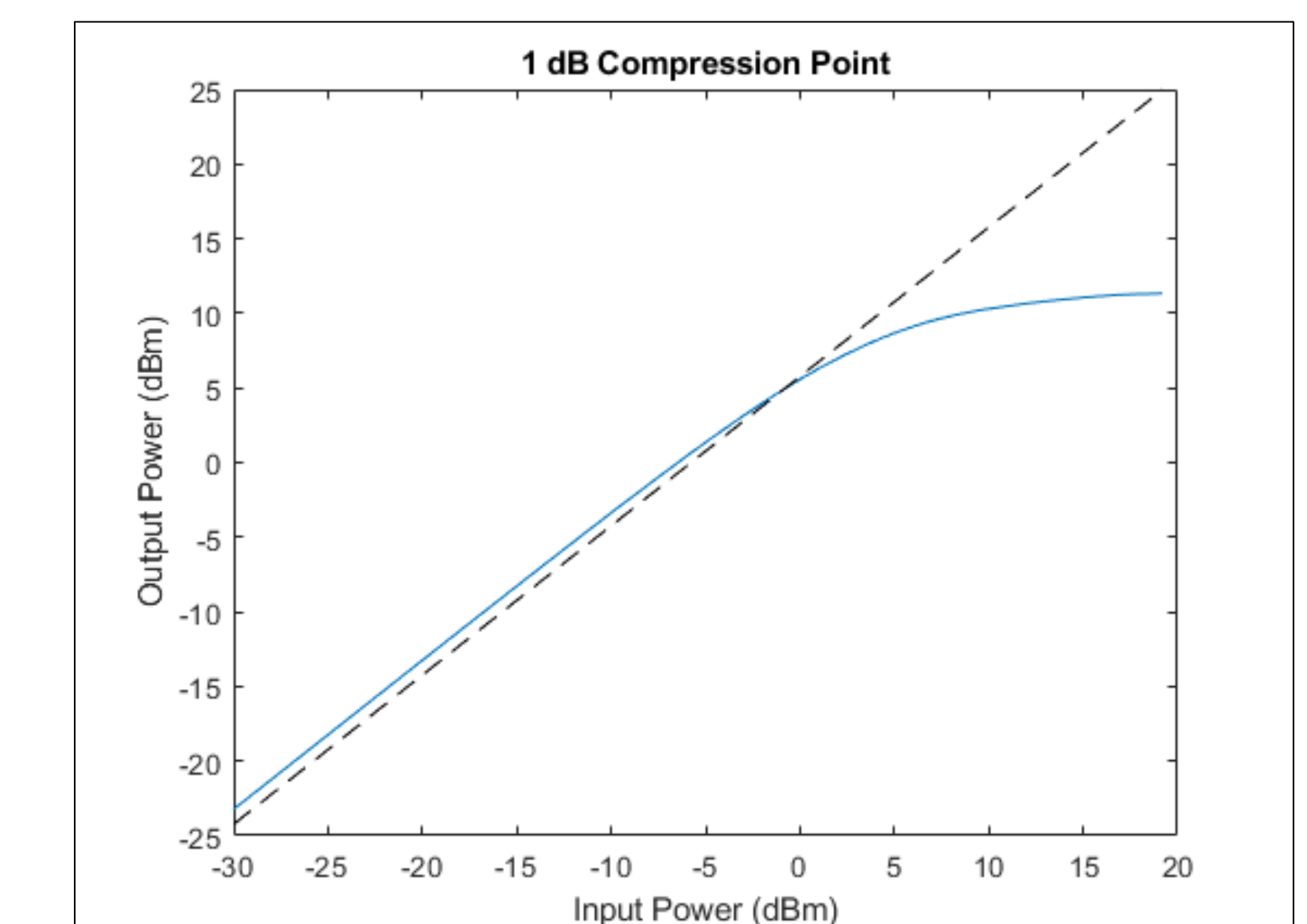
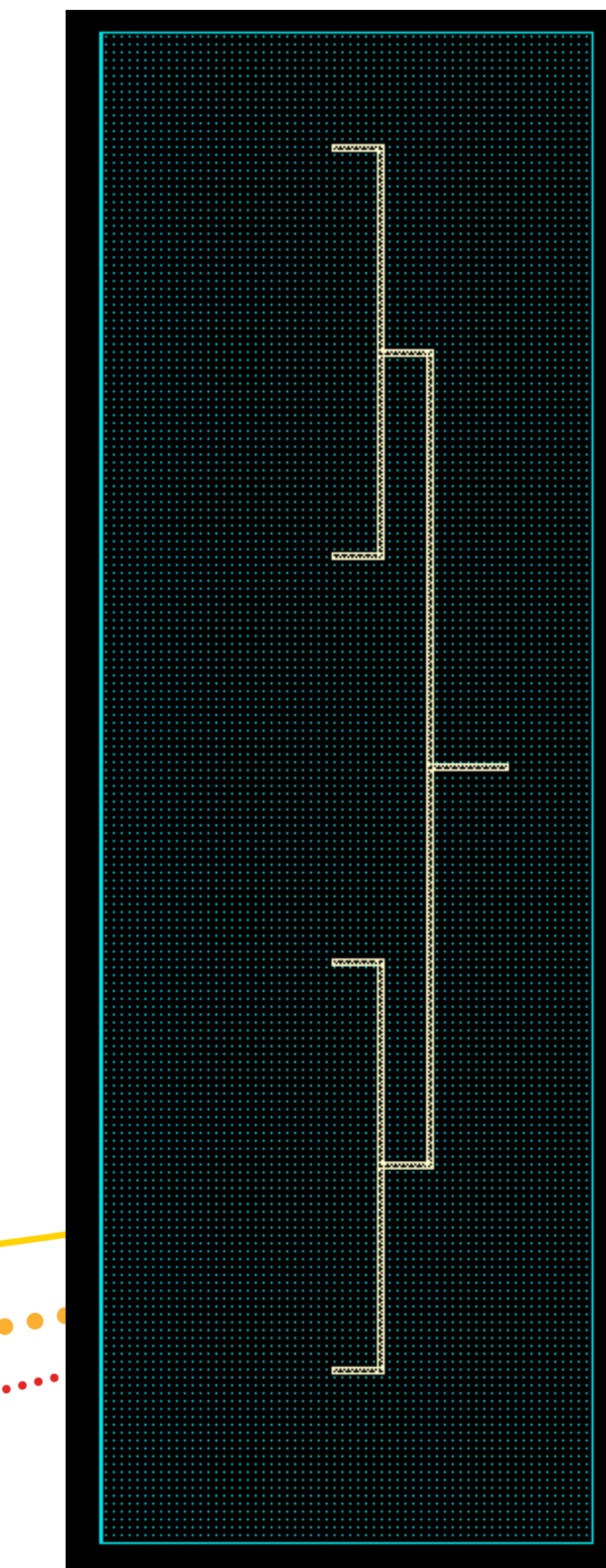


Figure 3: PA Survey [3]

