140 GHz Power Amplifier for 6G Applications

Final Design Report

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Glossary

6G - Short for sixth generation, referring to the next generation of mobile network after 5G

IoT - Internet of Things, computers and other computing devices that exchange information about the outside world

AI - Artificial intelligence, a method or algorithm used by computers to extract meaning and behaviour from information

VR - Virtual reality, a simulated environment that gives realistic impression of the real world

AR - Augmented reality, using elements of virtual reality overlaid on the real world

XR - Extended reality or “X” reality, umbrella term referring to the use of VR to varying degrees

mm-Wave - Millimeter wave (abv. mm-Wave) 30-300 GHz

THz, Terahertz - 0.3 to 3 THz or more broadly 0.1 to 10 THz

sub-THz - Sub terahertz, 100 to 300 GHz

CMOS, Complementary metal oxide semiconductor - a manufacturing process by which NMOS and PMOS transistors are integrated on the same circuit

III-V - Refers to semiconductors using groups III and V on the periodic table. Examples include InP (Indium Phosphide), GaN (Gallium Nitride), GaAs (Gallium Arsenide)

Direct conversion - a transceiver architecture where the signals are directly up or down converted to and from radio frequency (RF) with no intermediate frequency (IF)

System level - Understanding an engineering design made of abstracted blocks with emphasis placed on their behaviour rather than their internal operation

Executive Summary

The aim of this capstone project is to: (1) evaluate the suitability of the TSMC 65nm CMOS technology for millimeter wave applications, particularly wireless transmission, (2) model a wireless link for a next generation use case and determine suitable specifications for a power amplifier, (3) create a circuit level implementation and study the results. The 140 GHz band was chosen due to an industry consensus that moving to higher carrier frequencies will enable greater bandwidth which will be necessary to serve greater wireless throughput.[1] Typically, such high power, high frequency applications are implemented in niche, RF-centric technologies which are expensive and have low integration complexity. CMOS on the other hand may have worse RF performance but offers extremely high integration with digital circuits and low cost when manufactured at scale.[2] A single chip solution with digital and analog/RF circuits lowers costs and eliminates complexity caused by interfaces between disparate dies. This project successfully demonstrates a power amplifier in 65nm CMOS from 136 to 142 GHz (6 GHz bandwidth with 1dB gain flatness) which delivers up to 12 dBm to a 50 Ω load while consuming 240 mW of DC power from a 1.2 V supply with an area of only 0.3 by 0.3 mm^2. Such a power amplifier can enable wireless links with a range of up to 29 meters with a data rate of 7 Gbps.

Project Motivation and Objectives

Major technological trends are driving wireless networks towards sixth generation (6G) communications, including the internet of things (IoT), artificial intelligence (AI) as wireless users, and pervasive digital presence. These trends will push the total number of wireless devices in the world to over 500 billion in the next decade, demanding an order of magnitude increase in data throughput while decreasing network latency. [1] While human user experiences have defined the previous five generations of wireless networks, AI will soon have a presence as a legitimate user that far exceeds the perceptions requirements of human users. For example, AI systems could generate or demand machine vision data many times greater than the spatial or time resolution requirements for human-to-human video conferencing. [1] Emerging applications in "XR," which is a combination of virtual reality (VR), augmented reality (AR), and mixed reality (MR) will rely on much higher data rates than what is capable with 5G to provide truly immersive user experiences. Initial estimates put the minimum data rate for immersive 16K VR at approximately 1 Gbit/s for a single user, which is already the current experienced user data rate. [1]

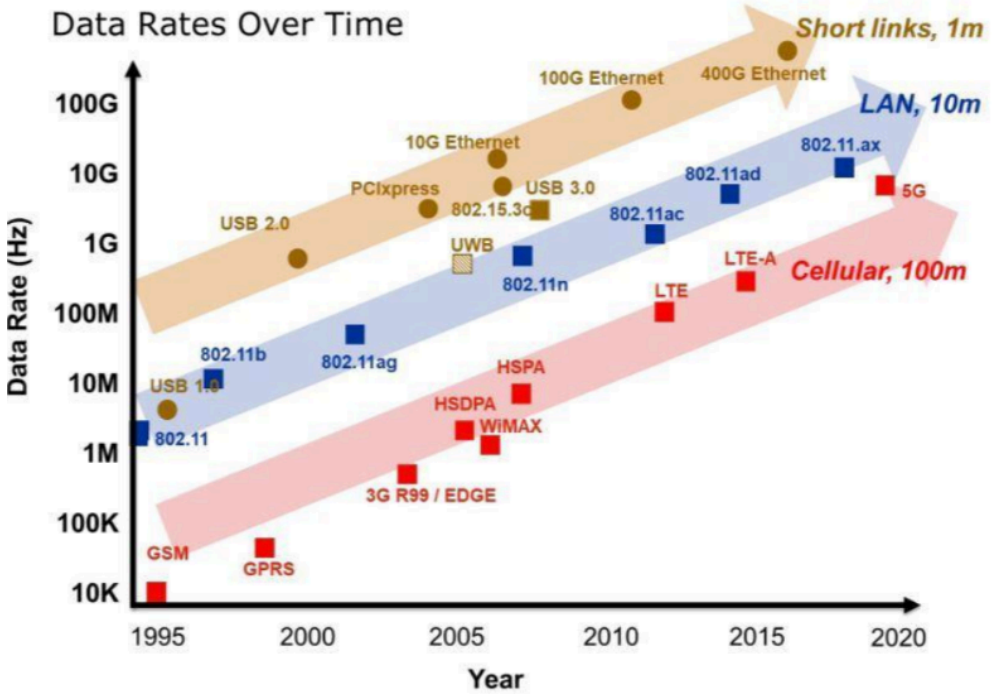

Figure 2. Data rates as function of time for wireline, short range wireless, and cellular communications. [2]

Currently, 5G will only serve as a stop gap on our way to exponentially increasing data capacity. To enable the growth of 6G, new hardware systems will have to be designed to support high frequencies and new ways of transmitting and receiving wireless signals. According to the Shannon capacity limit (1), to increase the maximum capacity of a wireless channel (C), the bandwidth (B) and/or the signal to noise ratio (SNR) must be increased. Increasing SNR usually involves increasing the power of the transmitted signal which becomes impractical as the improvement in C from SNR increases at a log rate. Not to mention limits on transmitted power and depending on the carrier frequency, fundamental limits of the transmitter technology compound its impracticality.

$$C = Blog_2(1 + SNR) \text{ (1)}$$

On the other hand, increasing bandwidth yields a linear increase to channel capacity. Due to a combination of physics and frequency allocations, shifting to higher carrier frequencies can provide orders of magnitude increase in bandwidth. Firstly, (2) illustrates that the bandwidth of a resonator is linearly proportional to the resonant frequency of the system. So simply by virtue of increasing the operating frequency in a conventionally tuned circuit, more absolute bandwidth is available.

$$B = \frac{f_c}{Q} \text{ (2)}$$

Recent regulation changes [3] have also opened up vast amounts of the radio spectrum above 100 GHz. Compared to sub-6GHz 5G networks and wireless LAN, the THz range (100 GHz to 10 THz) could enable a 50 to 100 fold increase in carrier frequencies and an associated 5 to 20 fold increase in available bandwidth. Going such high frequencies will require extensive design investigation for current integrated circuit (IC) technology, as common process technologies such as a complementary metal oxide semiconductor (CMOS) struggle to operate in this frequency range. Therefore the key enabling engineering solution that will enable 6G communication will be power amplifiers that can operate in the THz range with reasonable efficiency, reliability, and cost. The objective of this capstone project is twofold. Firstly, the efficacy of wireless

communications above 100 GHz will be examined and a series of technical specifications will be developed. Secondly, a circuit will be designed that satisfies these requirements and acts as a proof of concept technology for 6G on a physical level. By designing a low cost chip that can communicate in the THz range will support the exponential rise of data rate required, beyond what 5G can provide and enabling a whole host of exciting applications from enhanced autonomous vehicles to extending the presence of AI to everyday life.

Methodology and Design

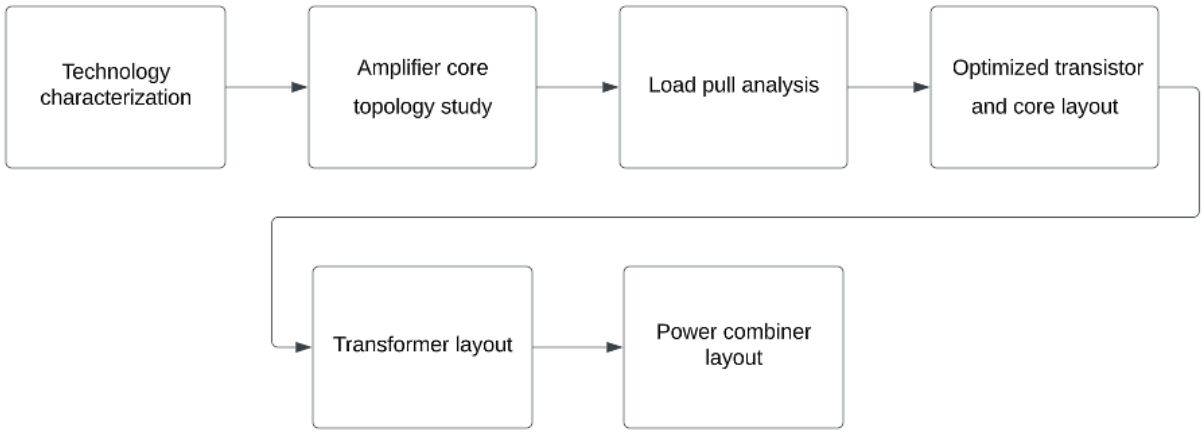

Figure 3. High Level overview of the workflow used to design a mm-wave power amplifier.

The first step to designing the power amplifier is to characterize the properties of the TSMC 65nm CMOS being used. This includes RF performance of the transistors at varying bias conditions and sizes, and passive structures such as transformers and transmissions.

Assuming the optimal current density for FET is relatively independent of the device width, the drain current of a minimum width NMOS device is swept to find the current density which results in peak fmax. Peak fmax is desirable as the device provides the most gain at high frequencies and the device can properly drive a load. Jopt is approximately 0.35mA/um in our chosen design kit. The total width and the finger width are then parameterized to find fmax a function of design dimensions with a constant Jopt. For a given total width, there is a finger width which minimizes gate resistance and maximizes fmax. All transistor finger widths were chosen based on the red optimal sizing line.

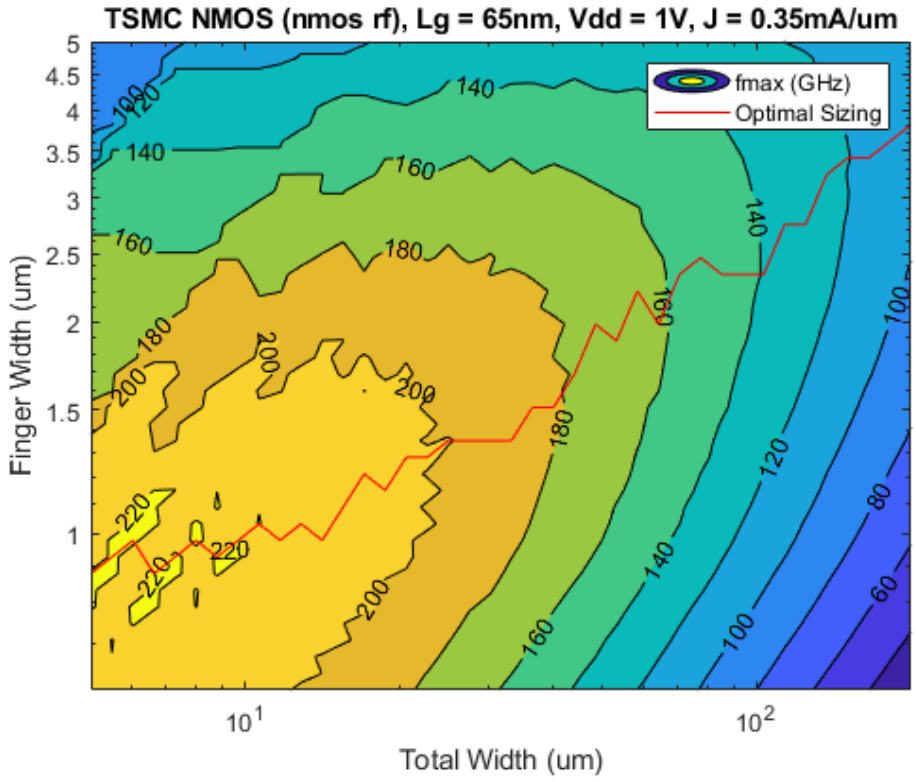

Figure 4. Fmax as a function of transistor width and finger width.

Practically speaking, the device width should not exceed 40 to 60 um to ensure an adequate amount of gain at 140 GHz.

A proof of concept transformer of diameter 30 um and trace width of 2um in the top two metal layers was implemented and simulated in EMX. The transformer shows results as follows: L1 = 35 pH, L2 = 40 pH, Q1 = 15, Q2 = 9, SRF ≅ 150 GHz, k = 0.7. The added loss of the secondary winding will be taken into account and the SRF of 150 GHz means transformers must be designed carefully such that the operation frequency does not lie too close to the SRF.

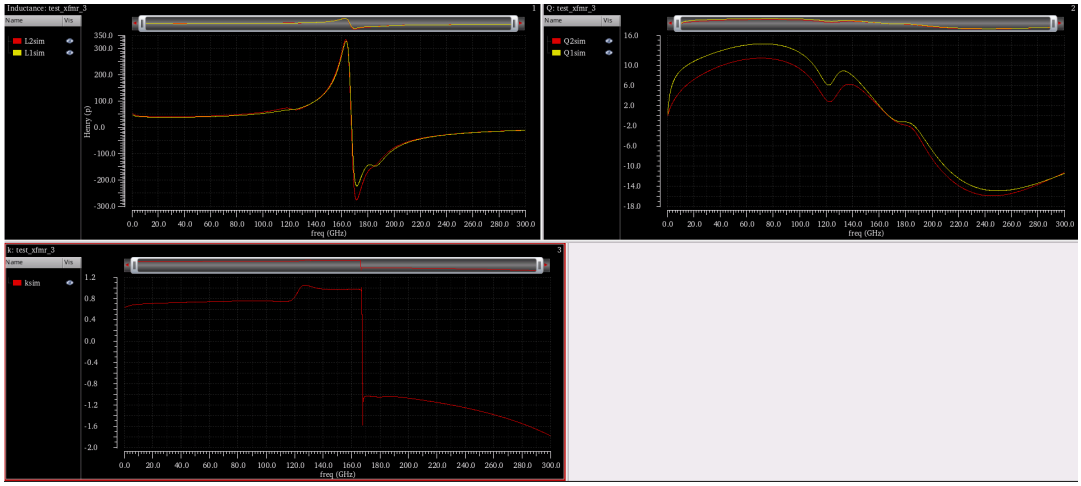

Figure 5. EM simulation of a proof of concept transformer.

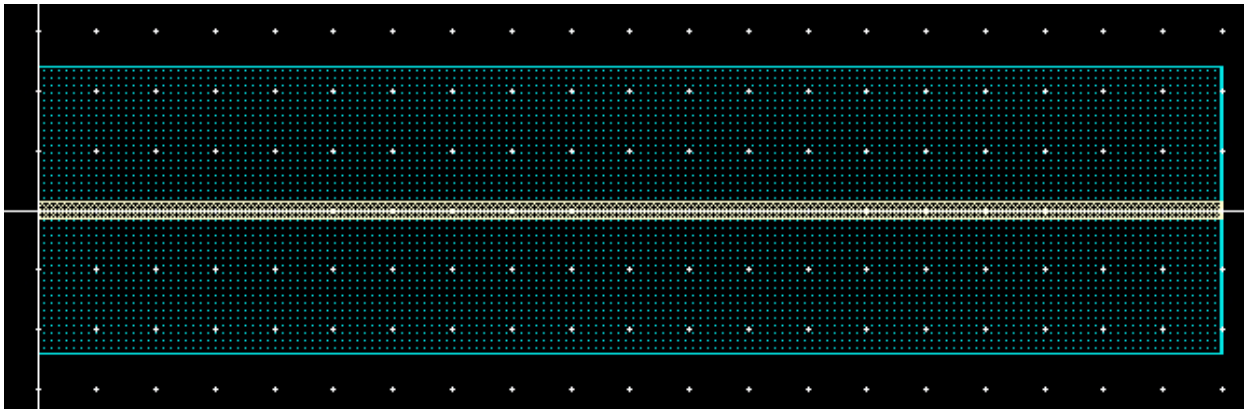

Figure 6. 100 um microstrip transmission line in metal 8.

Transmission lines will be used to facilitate power combining and short traces between components will also act as parasitic transmission lines. EMX simulations show that at 120 GHz, $\mathrm{re}\{Zc\} \leq 61.1\ \Omega$ in M9 while M8 can realize 50 and 71 Ω transmission lines. However, M8 is lossier with α~25 Np/m versus α~13.3 Np/m for M9. The wavelength for both transmission lines is approximately 1200 um. This will be used later to determine the physical size of the design.

In mm-wave CMOS amplifiers, it is common to unilateralize the core circuit to ensure stability and boost the (already limited) amount of gain in each amplifier stage. From a brief literature review, capacitive neutralization and inductive feedback are two possible options. Both methods require differential operation, which helps to suppress the 2nd harmonic and eliminates uncertainty in the ground signal return path. Capacitive neutralization is used in this design due

to its design simplicity and wideband operation when compared to the tuning required for inductive feedback.

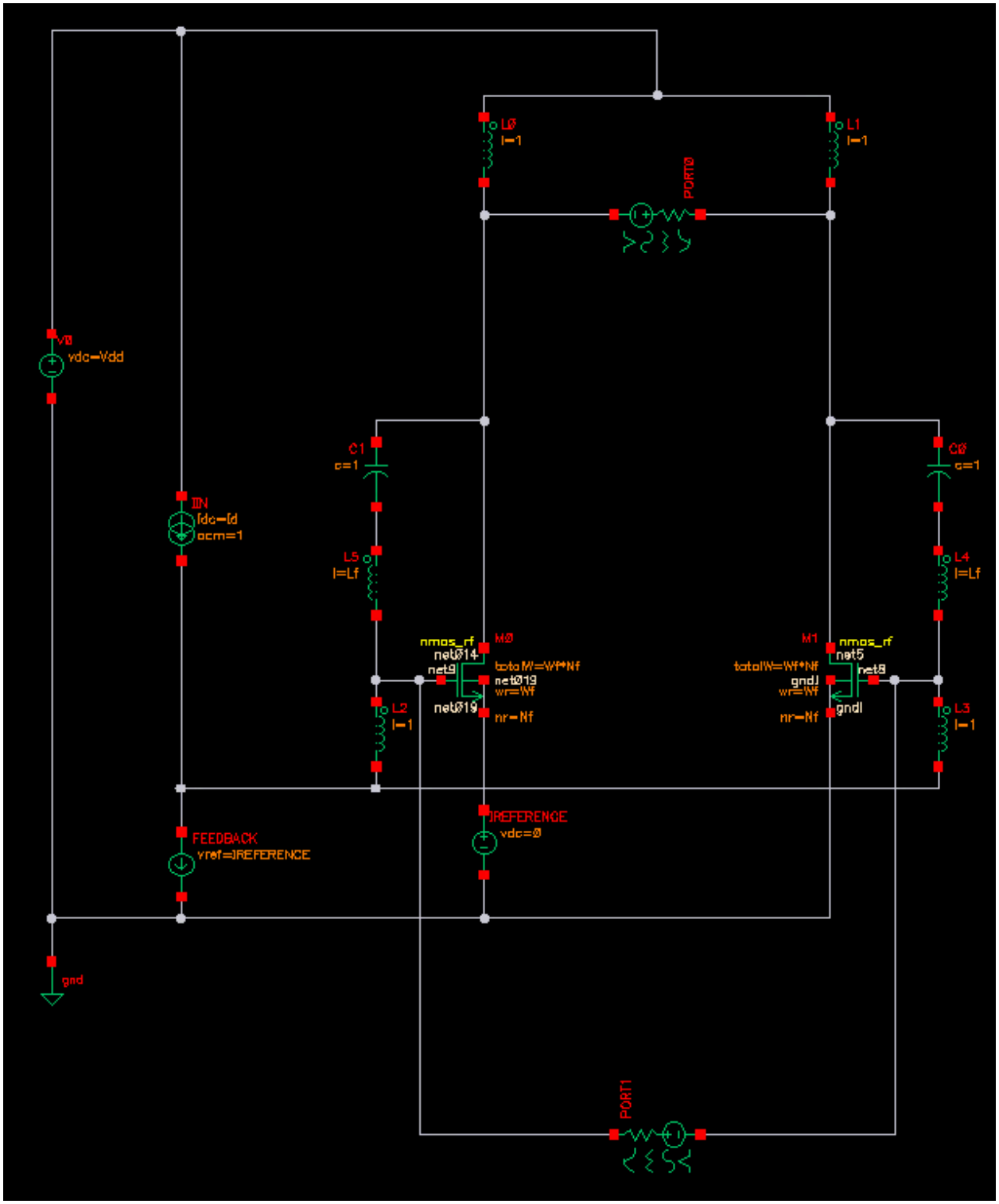

Figure 7. Amplifier core with inductive feedback.

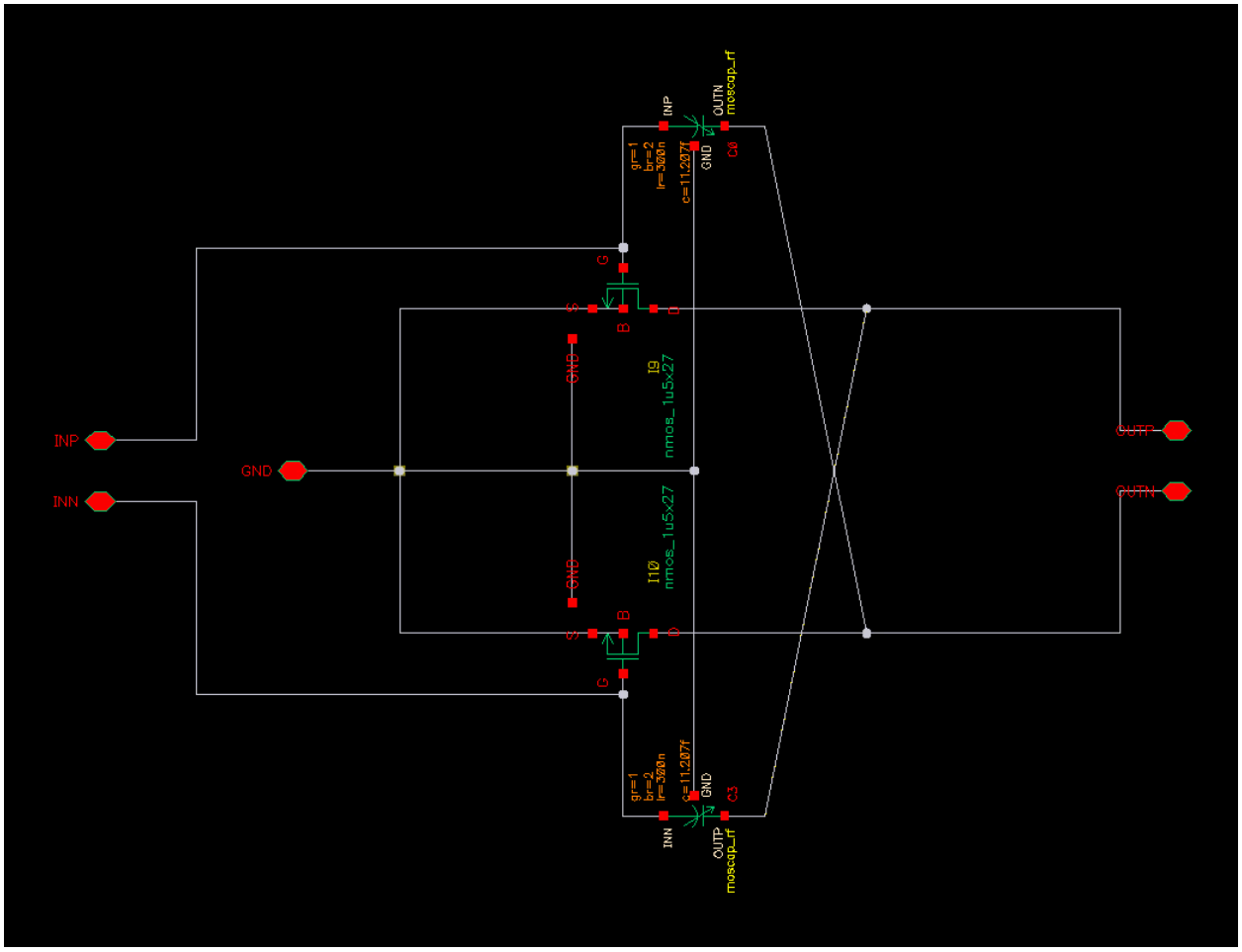

Figure 8. Finalized amplifier core with capacitive neutralization.

Once the amplifier core topology was chosen, a load pull analysis was conducted to determine the relationship between device width, power output, and the optimum load impedance. As the device width increases, Zopt decreases (with the real part shrinking faster than the imaginary part) and the power output and efficiency increases. At W = 50 um, the peak PAE suddenly decreases, which is likely due to uncertainties in the device model. Therefore the output stage was chosen to be W = 40 um to ensure the model was operating correctly.

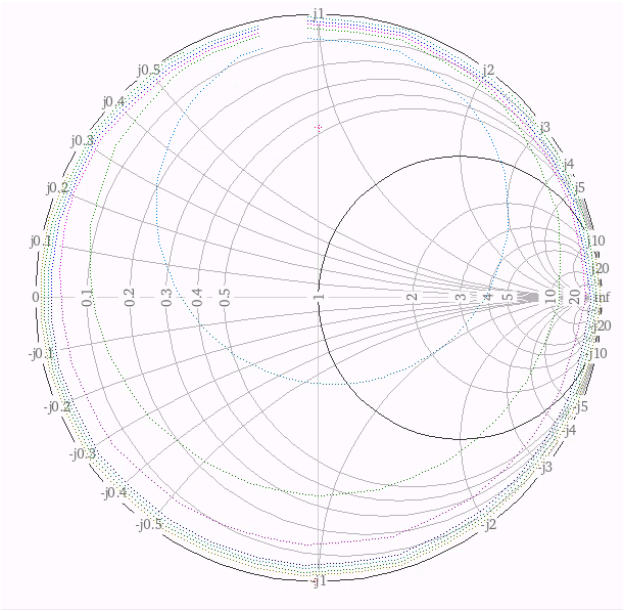

Figure 9. Constant power contours of a load pull analysis.

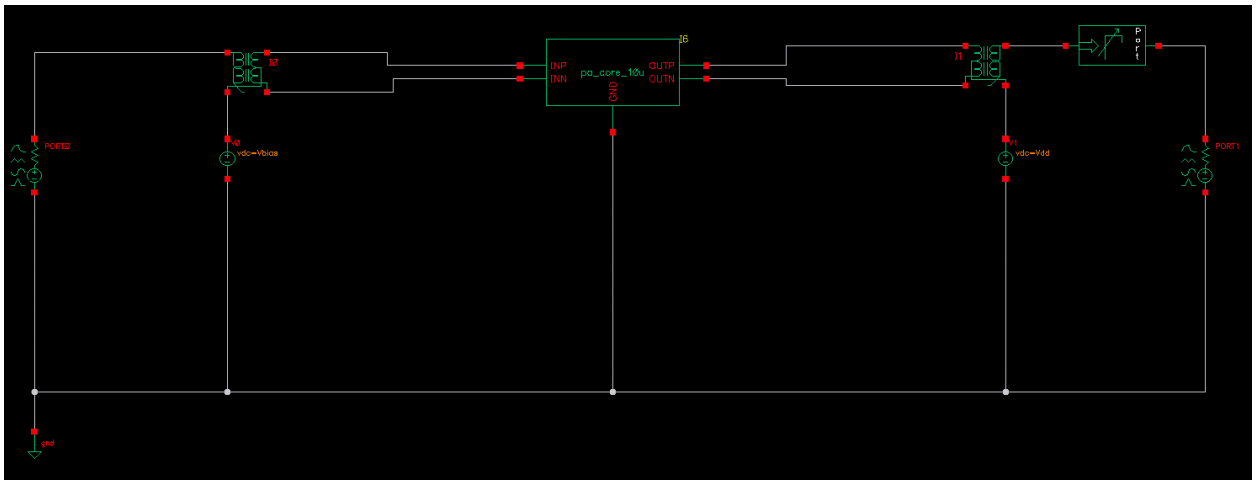

Figure 10. Schematic diagram of the load pull testbench.

Transistor Width (um)	Zopt (R+jX)	OP1dB (dBm)	Psat (dBm)	Peak PAE (%)
20	32+j89	6	10	37
30	24+j63	9	13	51
40	20+j46	11	14	57
50	24+j44	11.498	15	44
60	18+j33	13	17	59

Table 1. Output Stage Characterization, f = 120 GHz, Cneu = Cneu,opt

At the same time, the optimum neutralization capacitance was determined for varying device widths. There is a tradeoff between device width and gain. The predriver and driver stages favor smaller transistors for high gain whereas the output stage favors larger transistors for high power output. The 1.5 dB margin is used as an approximation for losses in the design. The neutralization was chosen to maximize the k-factor at 120 GHz.

Transistor Width (um)	Cneu,opt (fF)	GMAX (dB) Cneu = 0	GMAX (dB) Cneu = Cneu,opt	1.5 dB Margin (dB)
10	3.2	7.3	8.5	7.0
20	5.6	7.6	7.2	5.7
30	8.4	5.6	6.2	4.7
40	11.0	4.4	5.2	4.0
50	12.0	3.6	4.4	3.2
60	14.0	3.1	3.8	2.6

Table 2. Optimum neutralization, f = 120 GHz

From this, the amplifier is designed with three stages of widths 10, 20, and 40 um respectively.

The default RF NMOS layout from TSMC was optimized up to 30 GHz, and as such has a limited fmax and generally poor mm-wave performance. A custom transistor layout was created to minimize Rg, Cgs, and Cgd while also providing connections for the transformer matching network. The fmax of a 40 um NMOS increased from 170 to 220 GHz, leading to greatly increased gain at 140 GHz. The layout was simulated with EMX and the intrinsic transistor model was embedded inside an N-port network.

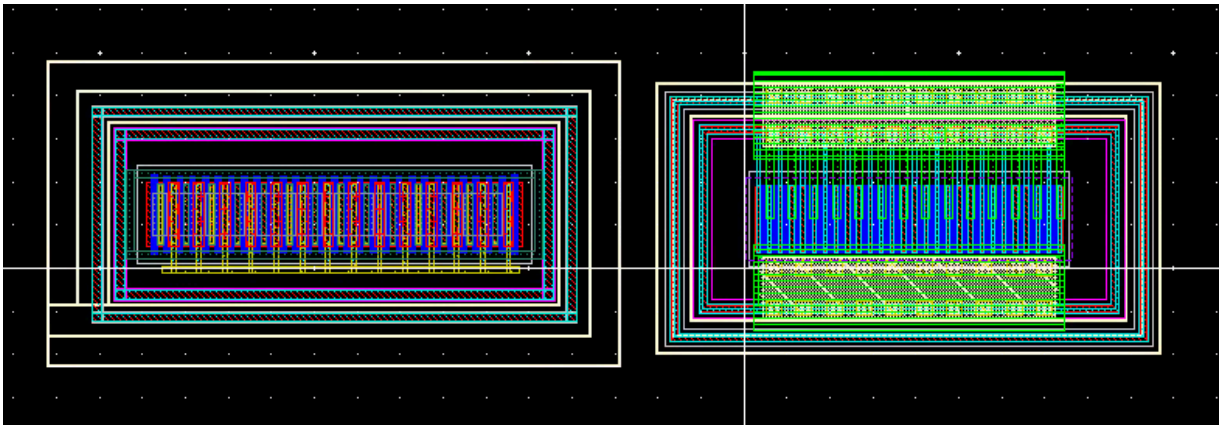

Figure 11. Left to right, TSMC nmos_rf layout, optimized transistor layout.

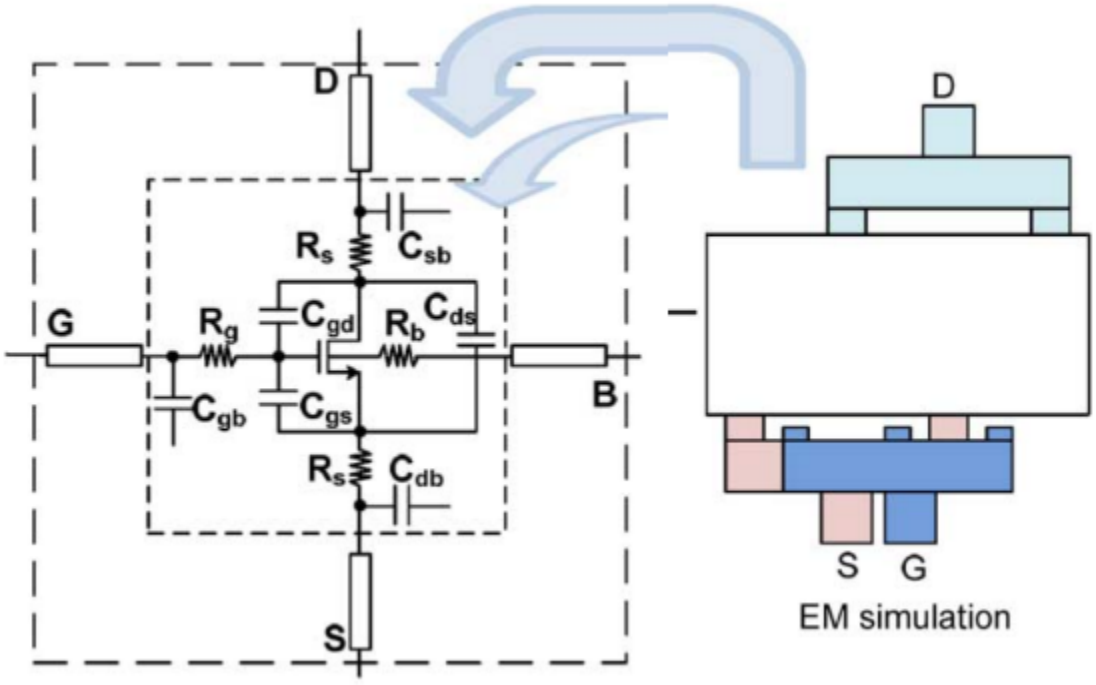

Figure 12. Transistor model embedded inside of an EM simulation. [10]

Once the optimized transistors were complete, the amplifier core layouts were created and simulated in EMX. The purple trace in Figure 12 shows the added transmission line effects from the EM simulation.

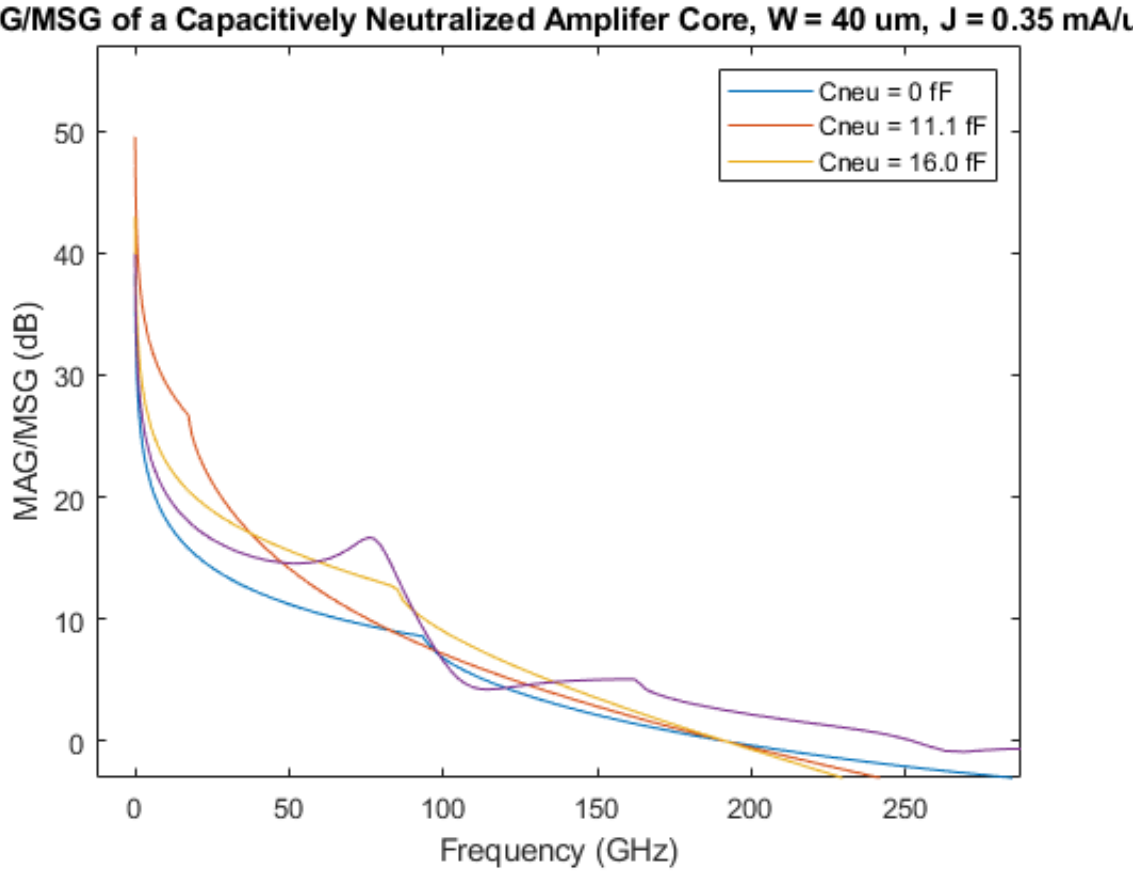

Figure 13. Transistor model embedded inside of an EM simulation.

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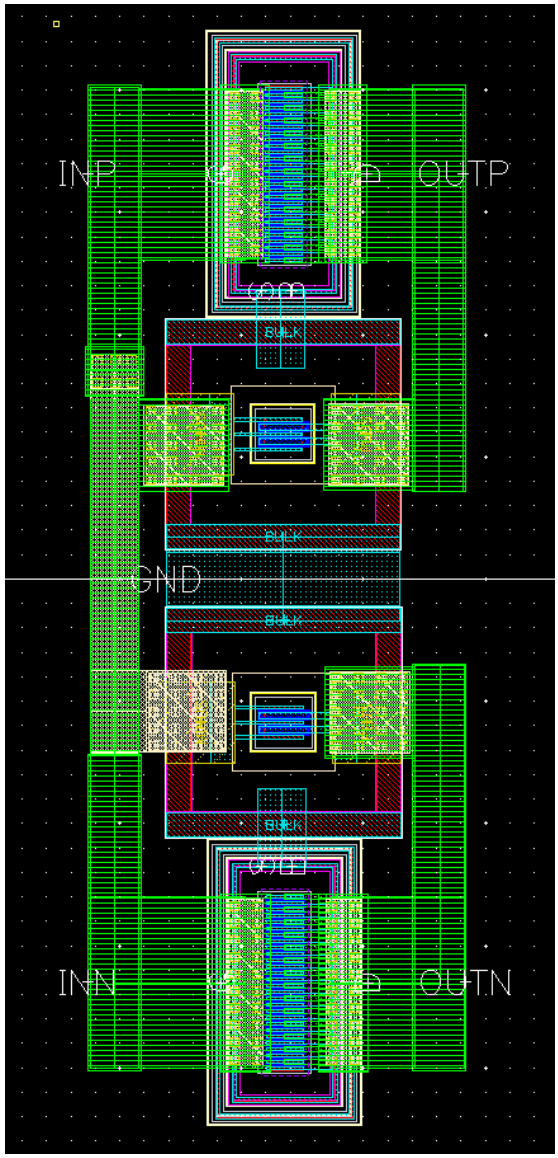


Figure 14. Amplifier core layout.

The completed amplifier cores were then assembled using ideal transformers as matching networks. Cadence's builtin optimizer varies the inductance of each transformer and its coupling coefficient to maximize the gain, ensure unconditional stability and load the output stage with the optimum output impedance. The values of each transformer were recorded in a table. Each transformer was then designed and simulated in EMX with the goal of getting as close as possible to the optimized values. An RF pad model was also generated to properly tune the transformers as if they were in a real chip.

Transformer #	Lp (pH)	Ls (pH)	k
1	53.6	116.4	0.45
2	116.4	76.4	0.26
3	69.2	37.8	0.26
4	59.4	58.2	0.45

Table 3. Cadence Optimization (Differential Mode)

Transformer #	Lp (pH)	Ls (pH)	k
1	57.1	120.7	0.53
2	117.6	72.1	0.28
3	70.3	39.7	0.23
4	57.6	58.1	0.74

Table 4. Realized Transformers for EMX (Differential Mode)

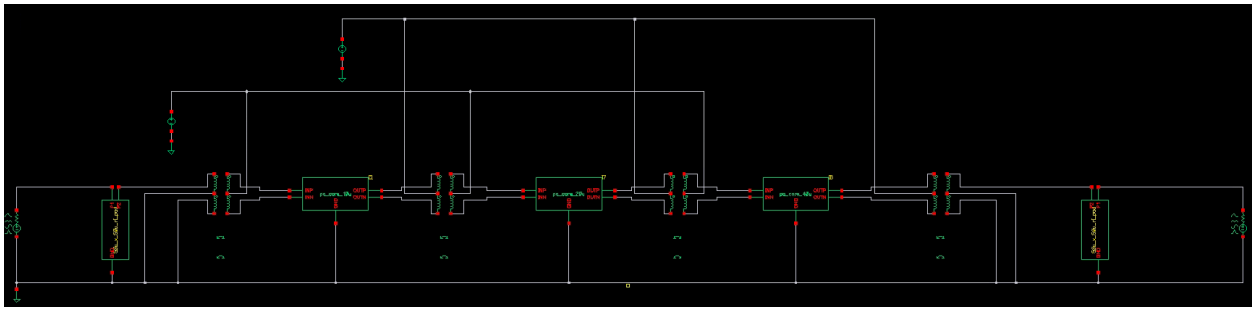


Figure 15. Complete 1-way amplifier with ideal transformers.

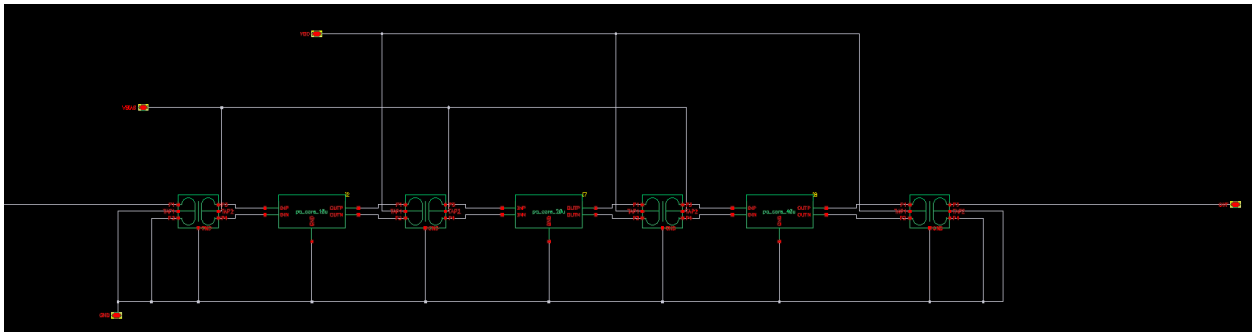


Figure 16. Complete 1-way amplifier with finalized transformer models.

Zero degree power combining was chosen due its simplicity, low loss, and minimal area. The power combiner and splitter are 4-way and are implemented in metal 8 with a 1.5 um width to achieve a 50 Ω characteristic impedance. The structure was simulated in EMX and an N-port s-parameter model was generated.

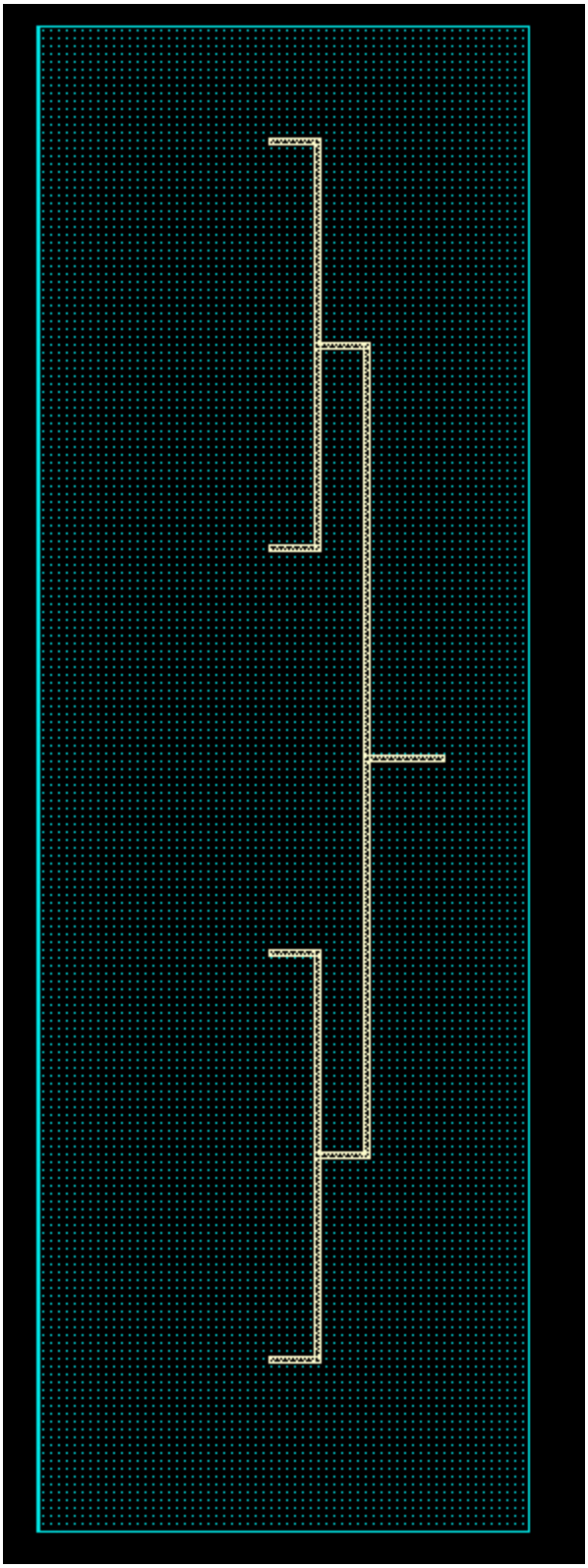


Figure 17. Zero degree power combiner.

Fig. 15. Zero degree power combiner.

The 1-way amplifier design is put into a separate cell and repeated as many times as necessary to connect to the 4-way combiner. The RF pads are also included to illustrate one possible implementation on a real chip.

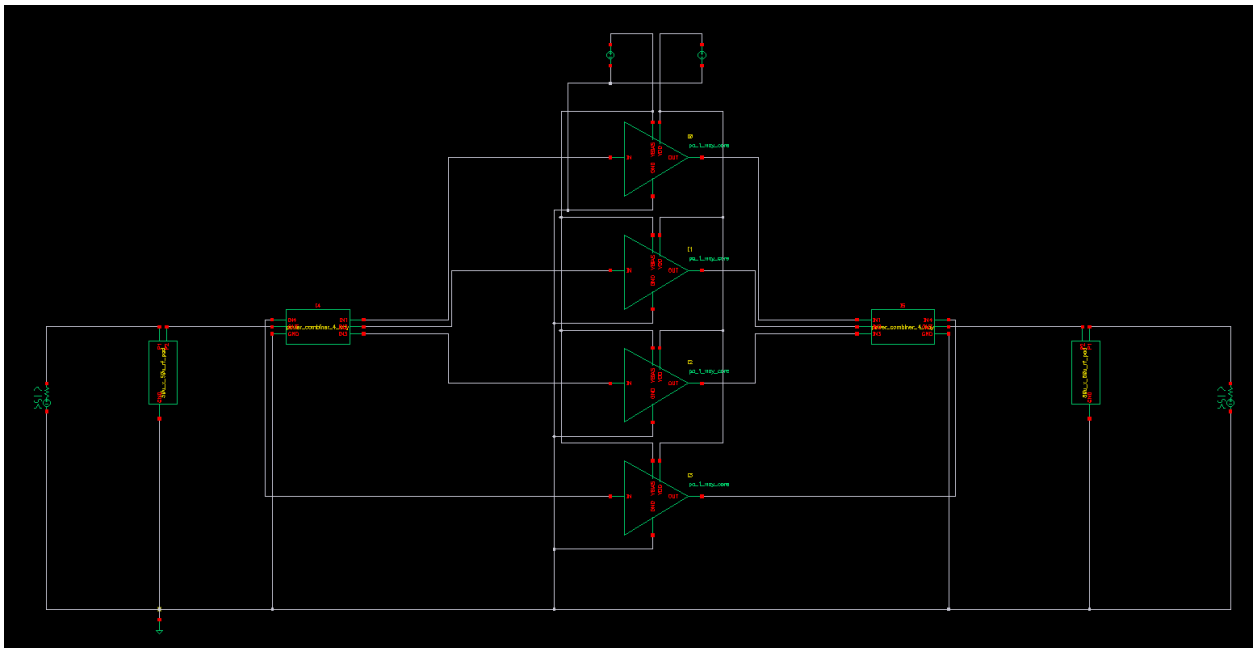


Figure 18. Schematic Diagram of the FInal Amplifier Design

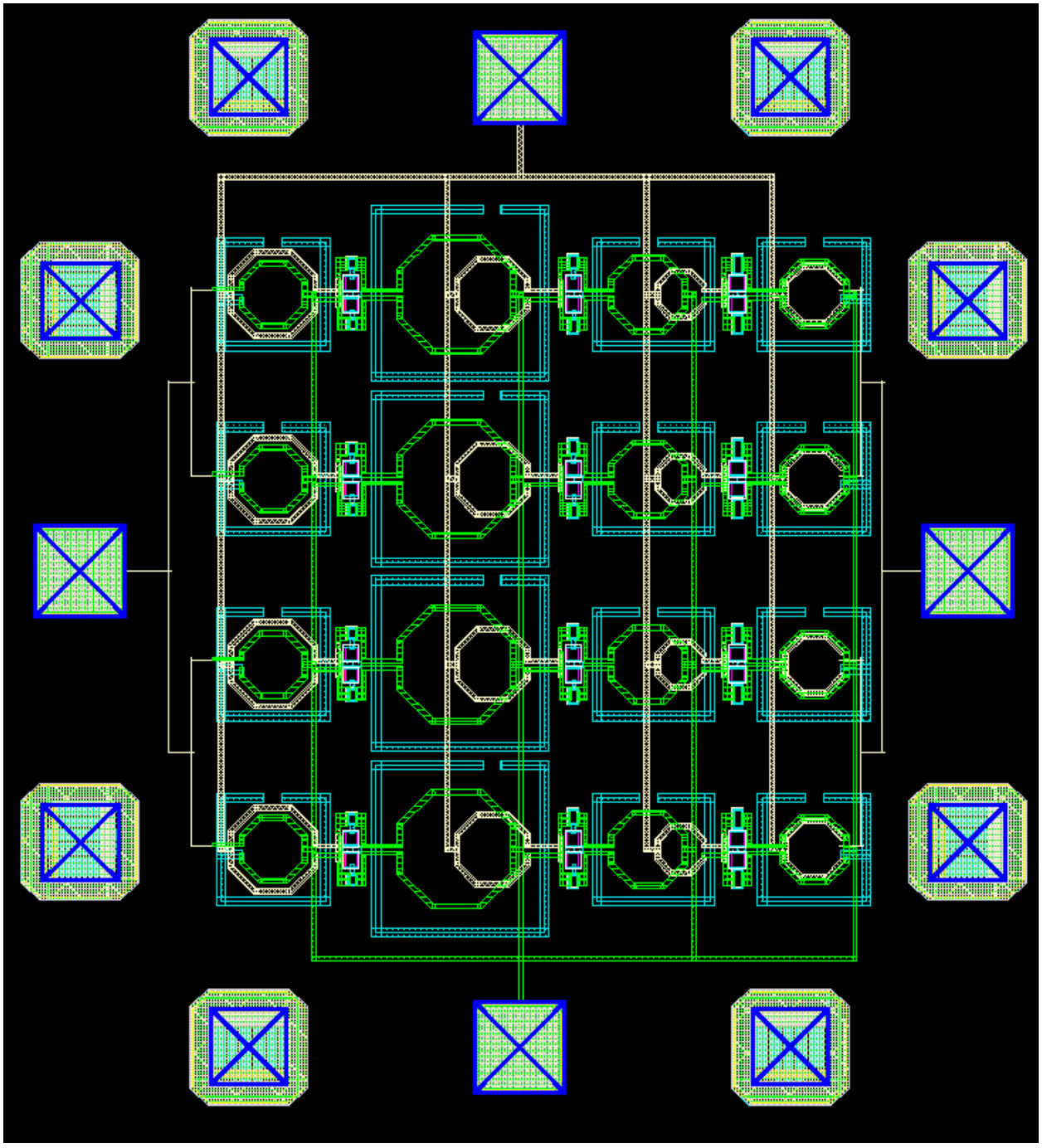


Figure 19. Layout of the Complete Amplifier Design

Product Scope and Functionality of the Final Product

To limit the scope and complexity of this capstone project to a reasonable degree, the design will be constrained to the transmitter power amplifier (PA) as highlighted in Figure 18. Focus for the design will be given to the power amplifier as its engineering is non-trivial and generating high power efficiently in the mm-Wave range (30-300 GHz) remains an open question ripe for experimentation. The power amplifier is responsible for taking the low power digitally modulated signal and increasing its power level so that it can drive an antenna and also performing the necessary impedance transformations to minimize reflections and maximize output power and efficiency. In this sense, the project only concerns itself with the power amplifier and not the RF chain precedes it, nor the antenna design that it would theoretically drive. The power amplifier is assumed to operate in a 50Ω environment, which is standard in microwave design.

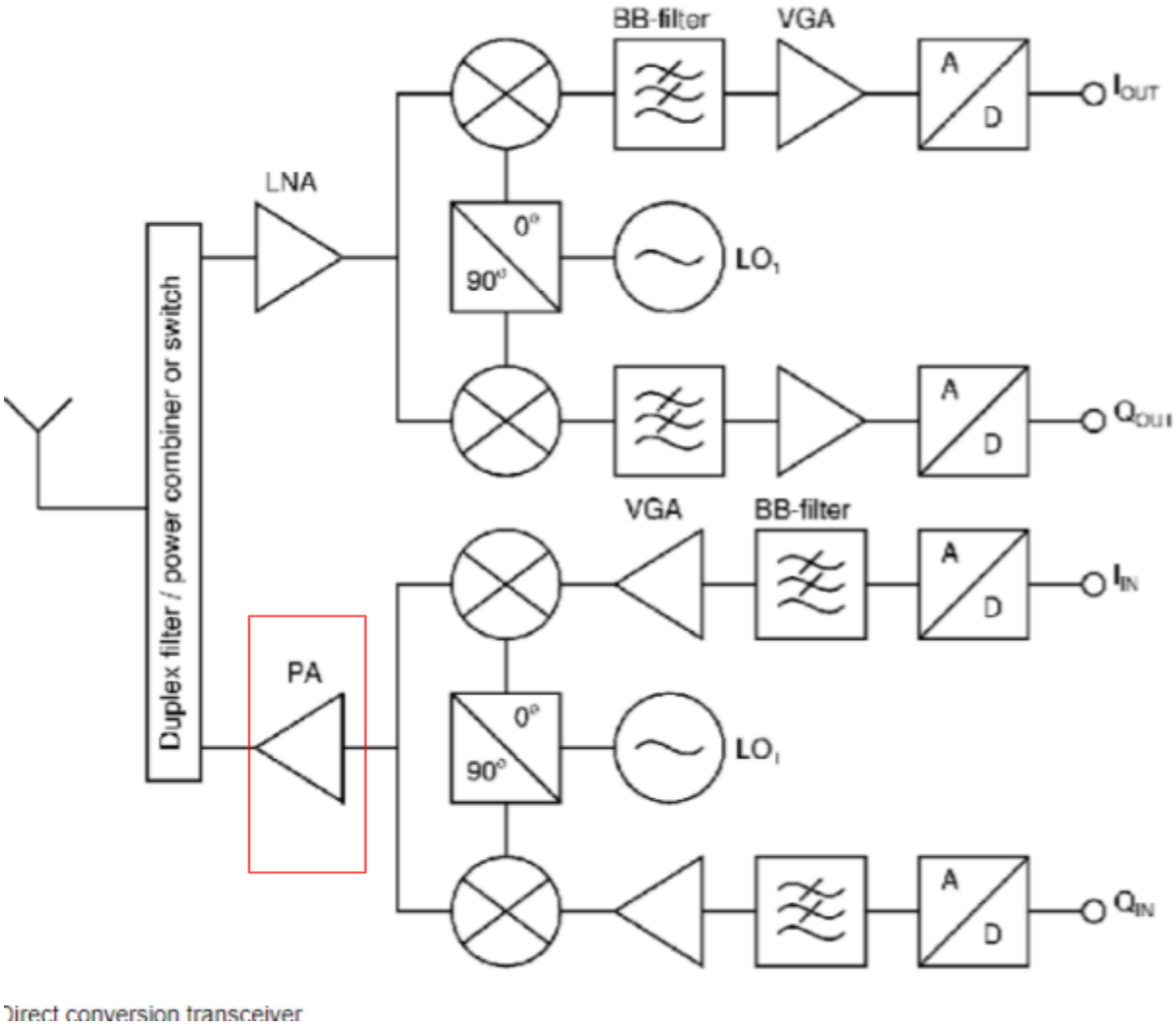
The power amplifier will be designed in a 65 nm CMOS process in Cadence Virtuoso firstly by schematic design, then layout, and finally post layout parasitic extraction. The must have deliverables are as follows:

- System level block diagram including the amplifier core, matching networks, power splitters, power combiners, and other relevant circuit blocks
- Basic analytical equations that model the 1st order behaviour of the chosen circuit topology and assist in sizing of components and biasing of active devices
- Circuit level schematic diagram showing components with relevant values/sizes
- Plots and summary table showing the two-port S-parameters of the post layout extracted circuit, gain compression, power consumption, efficiency and linearity across the band of interest
- Images of the final layout with appropriate annotations for each circuit block and die dimensions

In additional to the must have items are several should have items:

- A literature review of several power amplifiers in the 100 to 200 GHz range and a methodology for choosing the best topology/class of amplifier core
- Individual simulations of passive components, including inductors, transformers, power combiners, and power splitters
- A literature review of matching network schemes and power combining with simulations for each candidate

The final product remains consistent with the original scope of a mm-wave power amplifier. The amplifier consumes DC power, amplifies signals in the small signal regime, and outputs a high amount of power that is delivered to a 50Ω load. The amplifier operates in the specified frequency range and is unconditionally stable. The smith charts showing each impedance transformation were omitted from the final simulations, along with system level simulations with various digital modulation schemes. The optimization of the number of amplifier stages and combining ratio was kept to a minimum as opposed to the original goal of a fully fledged characterization due to time constraints.



Direct conversion transceiver

Figure 20. Block Level Diagram of a Direct Conversion Tranceiver with the PA Highlighted [4]

Technical Specifications of the Final Product

Technical Specification	Units	Target	Actual
Centre Frequency	GHz	119.5	138.8
1 dB Bandwidth	GHz	7	5.5
Frequency Range	GHz	116 to 123*	136 to 142
Psat	dBm	17	11.3
OP1dB	dBm	15	5
OIP3	dBm	-	20.2
PAE	%	10	1.7
Pdc	mW	800	244
S11	dB	-10	-11.6
S12	dB	-30	-42.3
S21	dB	10	6.77
S22	dB	-10	-11.4
Area	mm2	1	0.173
Technology	-	65nm CMOS	65nm CMOS
Supply Voltage	V	1 or 1.2	1.2

Table 5. Targeted and Simulated Technical Specifications

* Based on FCC spectrum horizons 2019 unlicensed band [3]

After careful consideration, the original specifications of the product were deemed too ambitious and not practical to achieve in 65nm CMOS. The actual technical specifications are representative of a compromise between small signal gain, DC power consumption, and saturated output power. The largest deviations from the original target at the centre frequency/frequency range and the saturated output power. Due to the low self resonant frequency (SRF) of the transformers, large inductances could not be achieved which set the centre frequency low enough to reach the original target. Instead, a 16% increase from 119.5 GHz to 138.8 GHz allowed the transformers to be small enough to remain in the first resonant mode. The losses in the transformer and the power combiner lead to a decrease in small signal gain from the target 10 dB down to 6.77 dB. The Psat of 11.3 dBm is significantly lower than than the target of 17 dBm, which is ultimately limited by the DC power consumption target and losses in the power combiner. 8-way and 16-way power combining may be able to achieve the desired Psat but the small signal gain will decrease to impractically low levels. The link budget calculation shows that the actual amplifier performance can still serve the original use case.

Measuring success and Results of Validation Tests

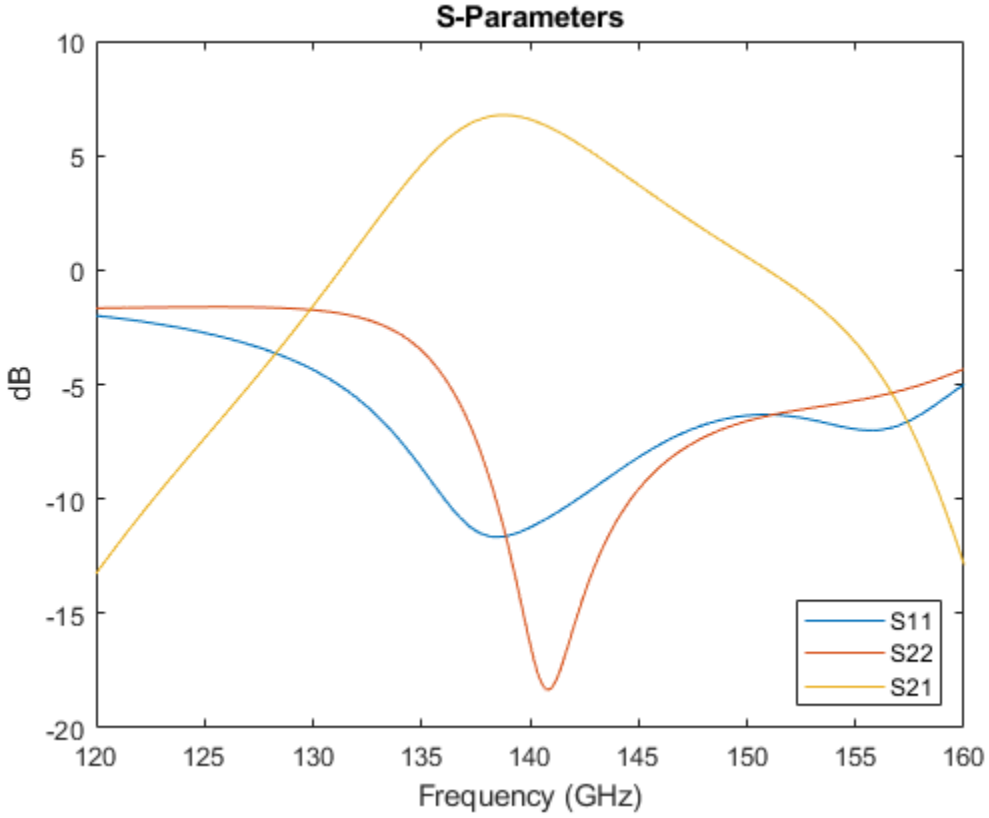


Figure 21. S-Parameters

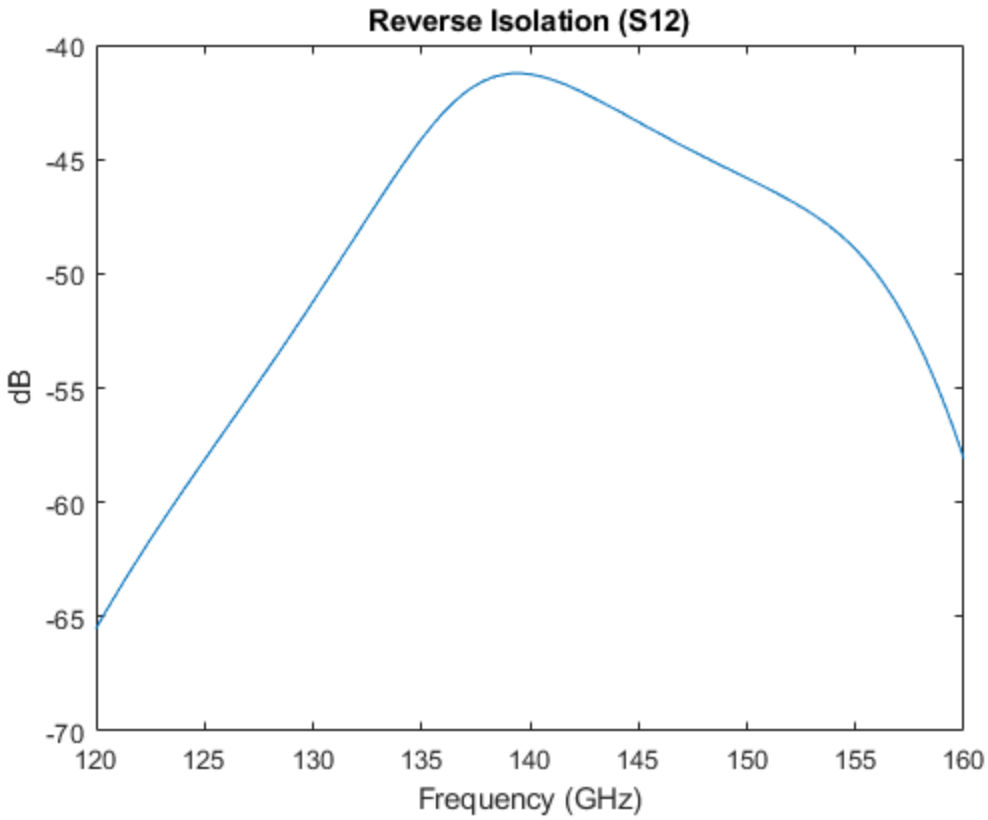


Figure 22. Reverse Isolation

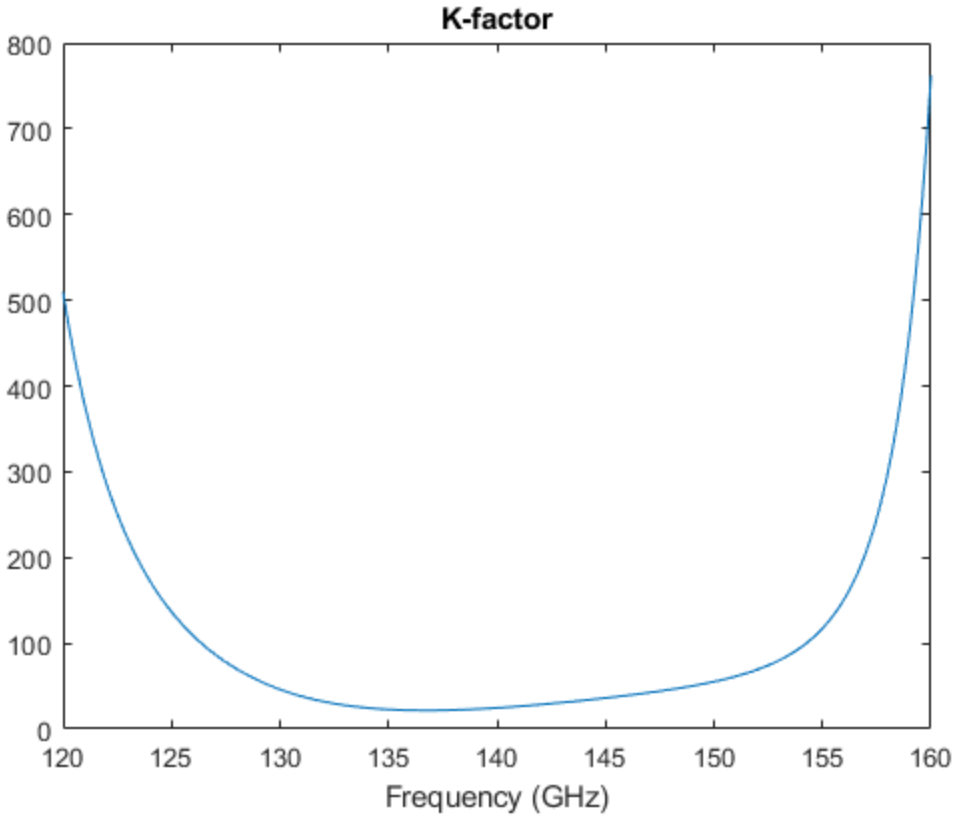


Figure 23. K-Factor

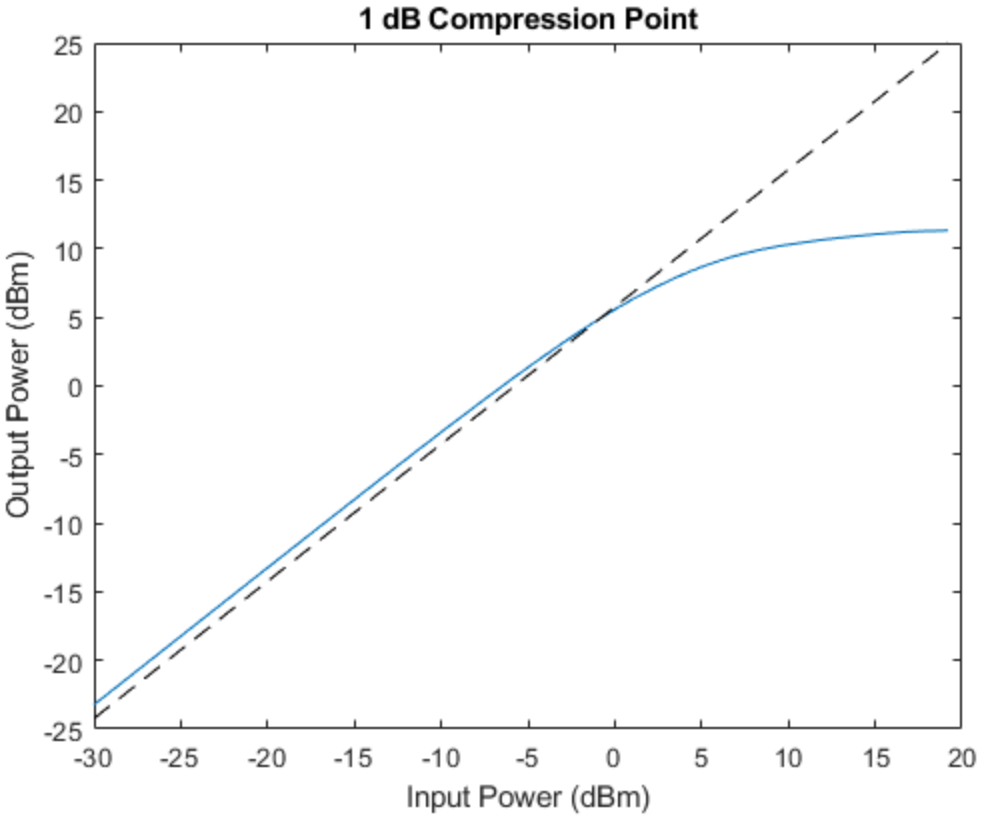


Figure 24. 1dB Compression Point

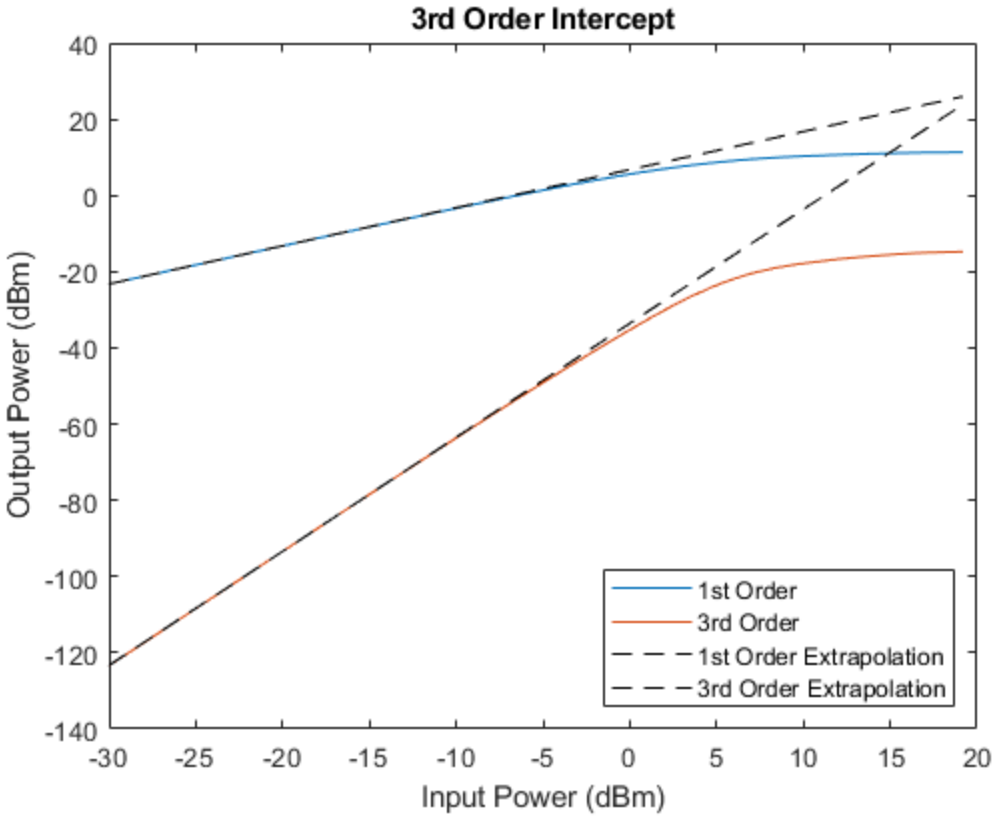


Figure 25. 3rd Order Intercept

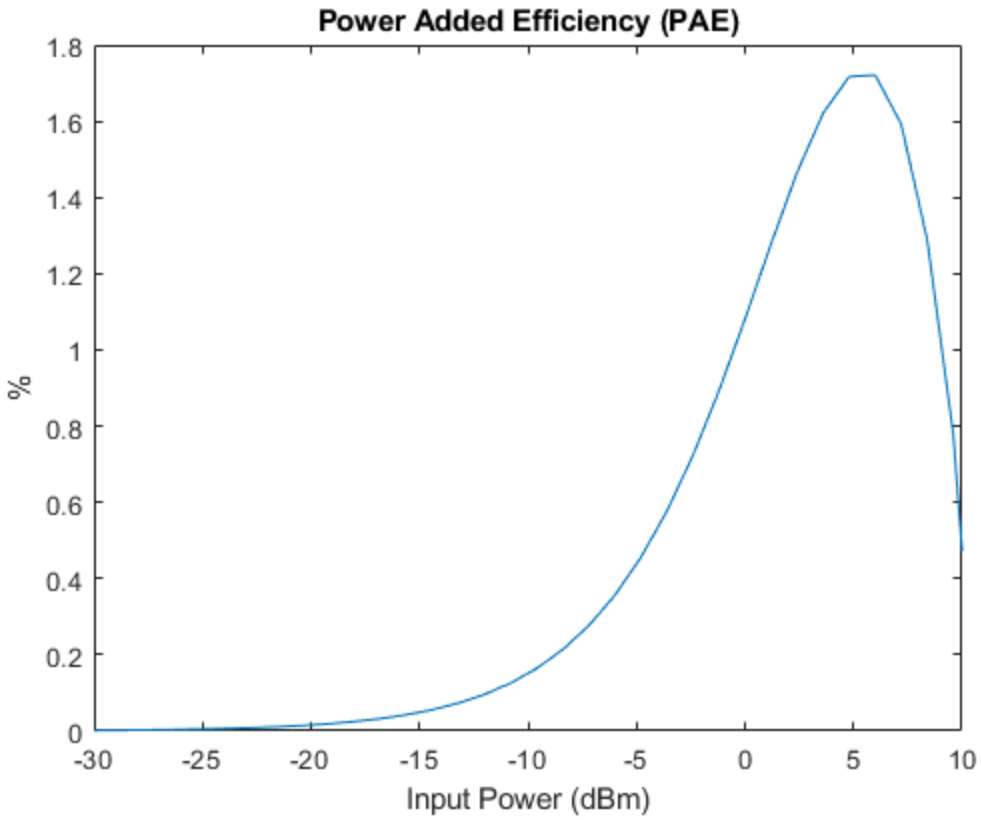


Figure 26. Power Added Efficiency (PAE)

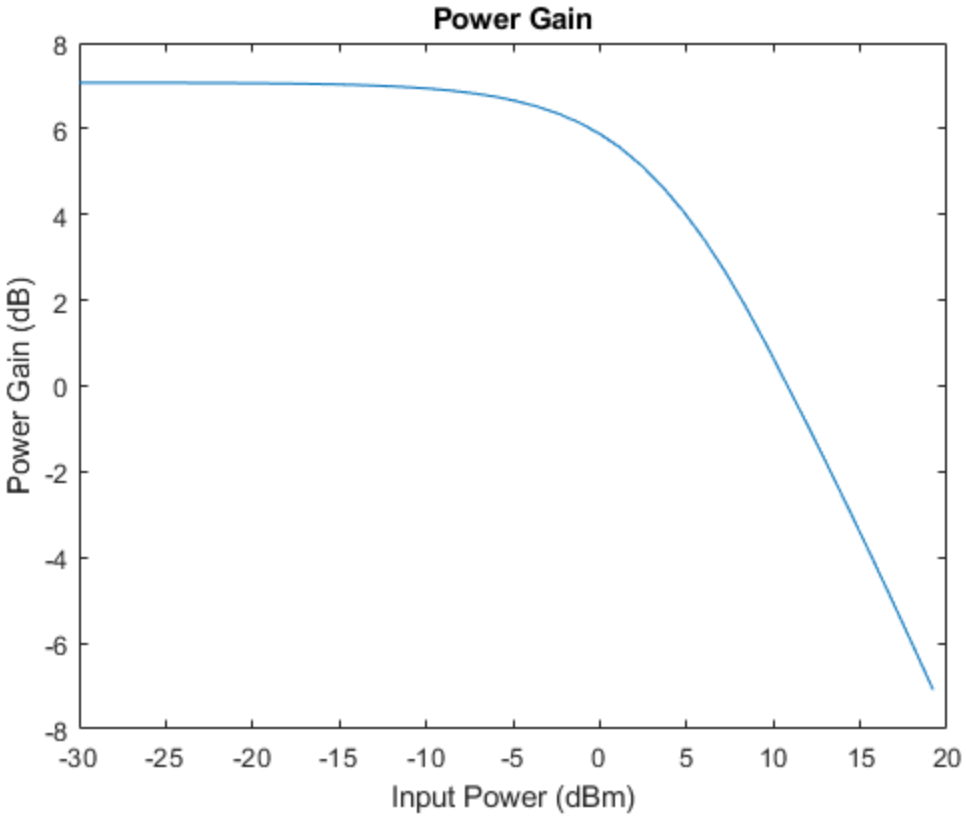


Figure 27. Power Gain

The complete amplifier simulated using the following analyses: DC operating point, S-parameter, and periodic state state. The DC operating point analysis confirms the bias point of the amplifier and gives the DC current consumption and by extension DC power consumption. The s-parameters show that the amplifier provides small signal gain at 140 GHz, the input and output match is acceptable and the reverse isolation is also acceptable. The k-factor calculator shows the amplifier is unconditionally stable over a wide range of frequencies. The periodic steady state analysis shows the amplifier has a linear region and saturates to Psat, which is the expected behaviour for a solid state amplifier. Also expected for a linear class A amplifier is the IP3 is well above P1dB and the power added efficiency reaches a peak close to the Psat level. Overall, these results show the amplifier can act as a suitable power amplifier in the 140 GHz range.

Project Management Reflection

Task	Planned	Actual	No of Days	No of Days Actual
Project Start	9/8/2022	9/8/2022	8	8
Initial Setup and Link Budget	10/31/2022	10/31/2022	54	54
System Specification	11/30/2022	11/30/2023	31	31
Schematic Design Iteration 1	1/13/2023	1/10/2023	45	42
Schematic Design Iteration 2	1/27/2023	1/20/2023	15	11
Schematic Design Iteration 3	2/10/2023	2/1/2023	15	13
Layout	2/24/2023	2/15/2023	15	15
Simulation 1	3/10/2023	2/20/2023	15	6
Simulation 2	3/24/2023	2/27/2023	15	8
Final Simulation	3/31/2023	3/8/2023	8	10
Project End	4/12/2023	3/22/2023	13	15

Table 6. Project Management Timeline

Upon comparing the actual project timeline with the planned timeline, it is evident that the team was able to complete all the tasks ahead of schedule, thereby giving more time for documentation and reflection at the end. Initially, the actual timeline was very closely followed to the planned, but later on the team demonstrated increased efficiency working together, tasks were completed expeditiously. The layout and simulation scrums, in particular, were executed with remarkable efficiency. The successful completion of the project within a shortened timeline is a valuable learning experience for the team, which will enable us to better plan future projects by allocating adequate time towards project definition and planning. This extra time also helped us to document and reflect on the project adequately. This achievement is a positive outcome that will benefit the team in future projects, providing ample opportunities for continued growth and development.

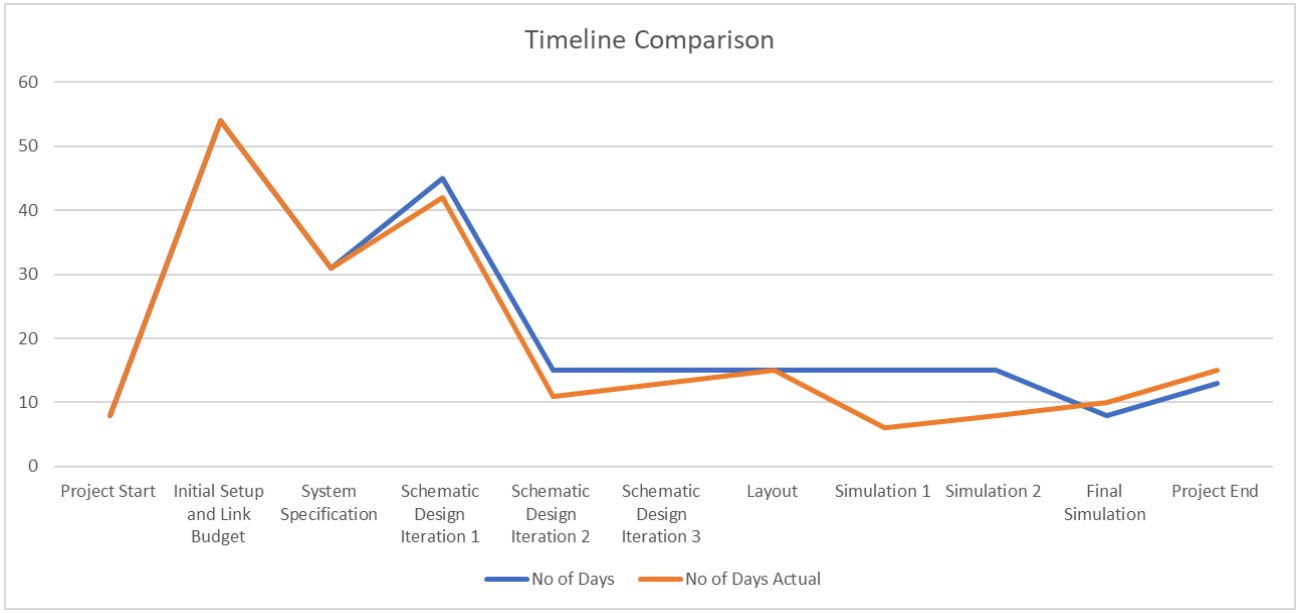


Figure 28. Timeline Comparison - Days

List of Tools, Materials, Supplies, Costs, etc.

The majority of this project was done using software based design tools, accessed through student licensing programs. Financial costs for this project arose for presentation purposes, and ease of use in the form of Presentation and note taking materials. The following table details products used throughout this project:

Tool/Material	Cost	Purpose
Cadence Virtuoso	$0	● Schematic Design ● Layout Design ● Layout Simulation and testing (LVS, DRC, EM)
Keysight Advanced Design Studio	$0	● Transformer sizing and simulation ● S-Parameter simulation
Mathworks Matlab	$0	● Design Calculations
Microsoft Office	$0	● Design Calculations ● Documentation
Google Workspace	$0	● Documentation ● Information Storage and Centralization
Zoom	$0	● Team Meetings
Discord	$0	● General team communication and coordination
Whiteboard Markers	$15	● Team Meetings
Poster	-	● Presentation
Plastic Filament	-	● 3D Printing Material

Table 7. Products Used

Reflecting on the limitations imposed by the COVID-19 Pandemic

During the 2022-2023 Academic year, COVID-19 precautions in Alberta had been reduced or phased out in prior months. As such, our team was free to conduct our weekly meetings in person, and coordinate through a mixture of in person and online communication. As a precaution, all meetings did have an option to join in online, if needed due to sickness or other extenuating circumstances. Our room bookings were made with call-in functionality in mind, and white board materials had heavy preference towards using personally owned markers and erasers over the publicly accessible tools. In this way, we attempted to mitigate any possible infection or spread of sickness.

Another possible concern that was discussed was the impact of supply chain on our product. With cases spiking in China and its surrounding area, any required shipping or materials would require increased timelines. Much of the material we would theoretically require for this type of design would be most easily sourced from this region, however ultimately costs would have been prohibitive to obtain required permissions and lisence materials and facilities for a physical implementation of our design. As such, this did not pose a significant limitation to our project.

Appendix

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